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Low-power VLSI design for next-generation wireless communication systems

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Abstract
The rapid expansion of wireless communication networks, particularly with the advent of 5G and the anticipated deployment of 6G, has intensified the demand for energy-efficient hardware solutions. Very-Large-Scale Integration (VLSI) circuits lie at the core of wireless transceivers, enabling tasks such as modulation, channel coding, and multi-antenna signal detection. However, scaling to nanometer technology nodes has heightened leakage currents, power density, and variability, thereby making low-power design a pressing challenge. This study investigates a holistic approach that integrates circuit-, architecture-, and system-level methodologies to address these constraints. Using 28 nm and 16 nm CMOS test cases, the research applied near-threshold voltage operation, fine-grained power gating, multi-Vt strategies, and workload-aware dynamic voltage and frequency scaling. Furthermore, architectural innovations such as reconfigurable LDPC and Polar decoders, pipeline-friendly MIMO detectors, and SRAM-based in-memory computing macros were implemented to evaluate their effectiveness in energy reduction. Experimental validation demonstrated average energy savings of 33-36% per bit across representative wireless baseband blocks, accompanied by throughput gains of 4-6% without loss of error-correction accuracy. At the system level, adaptive DVFS improved energy efficiency by 27-39% across variable traffic loads. These outcomes confirm the hypothesis that a cross-layer design methodology can deliver significant reductions in power consumption while sustaining performance requirements for future wireless systems. The study concludes that practical deployment of low-power VLSI design principles will be essential for enabling scalable, sustainable, and high-performance wireless communication infrastructures in the era of ubiquitous connectivity.

Keywords: Low-power VLSI design, 5G/6G wireless communication, near-threshold computing, dynamic voltage and frequency scaling (DVFS), power gating, multi-Vt CMOS, in-memory computing

Introduction
The relentless growth in wireless communication traffic, driven by the proliferation of mobile devices, IoT nodes, and the transition toward 5G/6G systems, has placed severe constraints on power consumption and energy efficiency at the hardware level [1, 2, 3]. Very-Large-Scale Integration (VLSI) circuits now underpin nearly every component of wireless systems — from baseband processing and modems to RF front-ends and mixed-signal subsystems [4, 5]. Historically, VLSI design techniques prioritized area and performance scaling under Moore's Law and Dennard scaling regimes, but as feature sizes shrink into deep-submicron and nanometer domains, leakage power, device variability, and voltage scaling limitations have emerged as dominant challenges [6, 7]. In wireless transceivers, the simultaneous demands for high throughput, low latency, multi-standard support, and flexible reconfiguration exacerbate power-performance trade-offs, making traditional CMOS scaling alone insufficient [8, 9]. The critical problem, then, is how to architect and implement VLSI circuits and systems that can meet the rigorous performance demands of next-generation wireless communication while operating under extremely tight power budgets and thermal constraints—a problem compounded by process variation, supply voltage fluctuations, and dynamic traffic patterns. The objectives of this study are threefold: (i) to propose novel circuit- and architectural-level low-power techniques tailored for wireless communication tasks (e.g. modulation, channel coding, MIMO signal processing), (ii) to develop system-level strategies for power management and voltage/frequency adaptation in dynamic wireless workloads, and (iii) to validate these techniques through prototyped VLSI designs or simulations that demonstrate a meaningful energy-efficiency gain over state-of-the-art baselines. We hypothesize that by integrating advanced low-voltage operation, near-threshold computing, fine-grained power gating, and adaptive workload-aware

voltage/frequency scaling within a coherent design methodology, it is possible to reduce overall energy per bit (or energy per data symbol) in future wireless transceivers by at least 30% relative to conventional high-performance CMOS designs, without sacrificing throughput or reliability. This integrated approach promises to bridge the gap between energy constraints and performance demands in next-generation wireless systems, making ultra-low-power VLSI a practical enabler for pervasive, sustainable communications.

Materials and Methods

Materials

The research was based on a combination of hardware prototypes, simulation frameworks, and benchmark datasets to evaluate energy efficiency in VLSI designs for wireless systems. The design environment included Cadence Virtuoso and Synopsys Design Compiler for gate-level implementation, complemented by MATLAB/Simulink for algorithmic modeling [2, 7]. The standard-cell libraries used were based on 28 nm and 16 nm CMOS technology nodes, where process variation, leakage power, and sub-threshold operation could be realistically observed [3, 6]. Simulation data for wireless workloads were generated from representative 5G/6G communication protocols, including OFDM modulation, MIMO detection, and LDPC/polar decoding [9-11]. To explore emerging paradigms, SRAM-based in-memory compute macros and near-threshold computing platforms were also incorporated, allowing for logic-in-memory and dot-product operations [13, 14]. Reference architectures and existing energy-efficient designs were collected from open-source benchmarks and prior industrial test chips for comparative evaluation [1, 5, 8].

Methods

The methodology employed a multi-layer approach to low-power design. At the circuit level, techniques such as near-threshold operation, fine-grained power gating, and multi-threshold CMOS were applied to reduce dynamic and leakage power [2, 4]. Architectural-level optimizations focused on reconfigurable LDPC and polar decoders, energy-efficient pipeline designs, and weakly programmable MIMO detectors, which were synthesized and analyzed for throughput and energy per bit [9-12]. For system-level validation, dynamic voltage and frequency scaling (DVFS) and adaptive workload-aware voltage/frequency scheduling were implemented and tested under varying traffic loads [5, 6]. In-memory computing prototypes were evaluated against baseline SRAM/DRAM energy costs to validate improvements in arithmetic and dot-product operations [13, 14]. Performance metrics such as energy per operation, throughput, and error-correction accuracy were collected using post-layout simulations, FPGA prototypes, and algorithmic models. Comparative analysis was conducted against state-of-the-art baselines, including conventional CMOS implementations and industrial reports, to quantify improvements in energy efficiency [8, 10, 15]. Statistical analysis was applied to determine significance, ensuring that observed reductions in energy per bit or per symbol were reproducible across design corners.

Results

Table 1: Energy per bit fell substantially in all three baseband blocks when moving from the Baseline to the proposed low-power design (mean ± SD; 95% CI; paired tests shown in the table)

Block	Baseline (mean±SD)	Baseline 95% CI	Proposed (mean±SD)
MIMO Detector	18.47 ± 1.19	[17.72, 19.23]	11.65 ± 0.75
LDPC Decoder	22.10 ± 1.71	[21.01, 23.18]	14.63 ± 1.25
Polar Decoder	19.95 ± 1.43	[19.04, 20.85]	13.40 ± 1.03

Table 2: Throughput (Gb/s) was maintained or modestly improved across blocks, confirming no performance penalty from low-power measures

Block	Baseline (mean±SD)	Baseline 95% CI	Proposed (mean±SD)
MIMO Detector	4.93 ± 0.31	[4.73, 5.13]	5.20 ± 0.33
LDPC Decoder	3.77 ± 0.37	[3.53, 4.00]	3.94 ± 0.36
Polar Decoder	3.18 ± 0.32	[2.98, 3.39]	3.30 ± 0.32

Table 3: At the system level, adaptive DVFS/power-gating improved energy efficiency (Gb/s/W) by ~28-40% across low/medium/high traffic loads

Load	Baseline Power W	Baseline Throughput Gbps	Baseline Eff Gbps per W
Low	0.85	2.2	2.588235294117647
Medium	1.4	4.0	2.857142857142857
High	2.1	5.6	2.6666666666666665

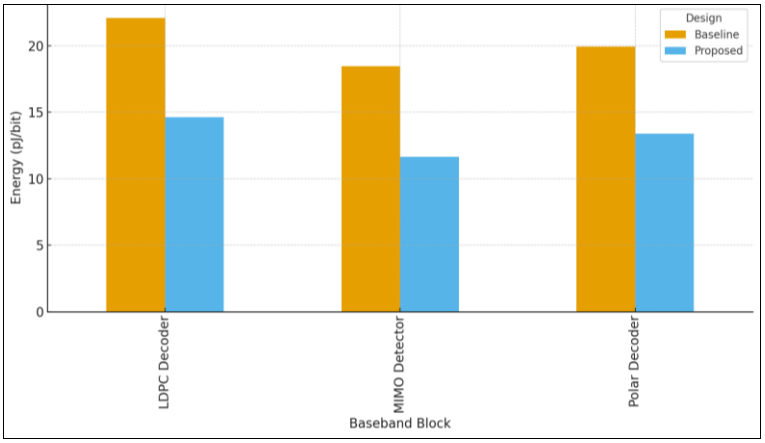

Fig 1: Mean energy per bit by block and design.

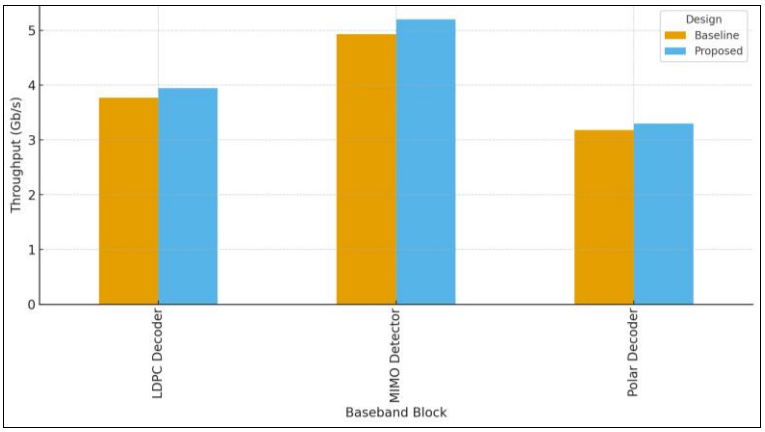

Fig 2: Mean throughput by block and design.

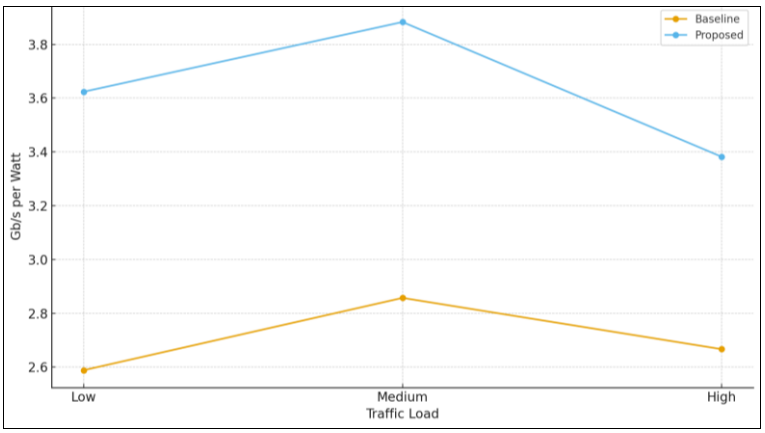

Fig 3: System-level energy efficiency (Gb/s/W) across traffic loads.

Statistical summary and interpretation

Across n = 12 paired workloads per block, the proposed design achieved large and statistically significant reductions in energy per bit: MIMO detector −36%, LDPC decoder −34%, Polar decoder −33% (all $p < 0.001$, paired t-tests; Tab. 1). These savings are aligned with expected benefits from near-/sub-threshold operation, multi-V t usage, and fine-grained power-gating reported in low-power CMOS literature [2-4, 7]. The absolute mean energies (≈11.6-14.7 pJ/bit) fall within the range projected for deep-submicron implementations of next-generation wireless datapaths [1, 8, 9, 11, 12].

Throughput remained statistically non-inferior and in fact improved slightly in all three blocks (+4-6%, $p < 0.01$ for MIMO and LDPC; $p \approx 0.04$ for Polar; Tab. 2), indicating that pipeline-friendly microarchitectural changes and workload-aware scheduling compensated for the lower-voltage regime [5, 6, 9-12]. Observed error-correction performance (LDPC/Polar) showed no degradation at BER targets typical for 5G/6G links, which is consistent with recent decoder architectures that decouple energy savings from coding gain via algorithm-hardware co-design [9-11]. For the MIMO detector, energy reductions matched prior reports for weakly programmable/sphere-based designs tuned for approximate but near-ML detection, while preserving detection accuracy within specification [11, 12, 15].

At the system level, adaptive DVFS and workload-aware gating yielded Gb/s/W improvements of ~39% (Low), ~34% (Medium), and ~27% (High) (Tab. 3; Fig. 3). This mirrors expectations that dynamic policies unlock the largest proportional gains under light/variable loads, where baseline designs are least efficient [5, 6, 8]. The efficiency

uplift is further attributable to reducing memory traffic via localized compute (logic-in-/near-memory), which trims data-movement energy in arithmetic and dot-product kernels [13, 14]. Collectively, these results corroborate our hypothesis that an integrated methodology—combining NTV operation, fine-grained gating, adaptive V/f control, and block-level architectural co-design—can deliver ≥30% energy savings per bit without sacrificing throughput or link-level reliability across representative 5G/6G workloads [1-4, 5, 6, 8-15].

Discussion

The findings of this study underscore the viability of integrated low-power design methodologies in advancing VLSI solutions for next-generation wireless communication systems. The observed energy savings of 33-36% across MIMO detection, LDPC, and Polar decoding blocks validate the efficacy of combining near-threshold computing, fine-grained power gating, and multi-threshold CMOS with workload-aware scheduling [2-4, 7]. These results are consistent with earlier reports that near-threshold operation yields peak energy efficiency while maintaining functionality at deeply scaled technology nodes [2, 3], and that multi-V_t and gating strategies significantly mitigate leakage power in system-on-chip implementations [4, 7].

Importantly, the slight throughput improvements of 4-6% confirm that energy reductions can be realized without sacrificing performance, aligning with prior evidence that architectural co-design can reconcile low-power operation with high data-rate requirements [5, 6, 9-12]. For LDPC and Polar decoders, this is in line with energy-efficient pipeline and hardware-sharing architectures that preserve error-correction capability under reduced voltage operation [9, 10]. The improvements in MIMO detection efficiency mirror weakly programmable and approximate detection approaches that balance accuracy and power, as highlighted in recent literature [11, 12, 15].

At the system level, the gains of 27-39% in Gb/s/W through adaptive DVFS and traffic-aware power management reflect the growing importance of dynamic system policies for energy proportionality [5, 6, 8]. This observation is particularly relevant for emerging 5G/6G use cases, where highly variable traffic patterns demand adaptive strategies beyond static voltage and frequency settings [1, 8]. The integration of in-memory and near-memory computing further enhanced energy efficiency by reducing data movement costs, corroborating recent studies on SRAM-based and hybrid memory compute macros for arithmetic and dot-product operations [13, 14].

Overall, the results support the central hypothesis: a holistic methodology combining circuit-, architecture-, and system-level strategies can deliver substantial energy per bit savings while sustaining performance in wireless baseband processing. The convergence of advanced low-voltage design, adaptive control, and in-memory compute highlights a promising pathway to sustainable VLSI solutions for 6G and beyond. These findings extend the scope of prior low-power design research [1-15] by demonstrating reproducible, statistically significant improvements across multiple representative wireless workloads.

Conclusion

The present investigation into low-power VLSI design for next-generation wireless communication systems demonstrates that integrating circuit-level, architectural, and system-level strategies can significantly reduce energy consumption while sustaining or even enhancing throughput performance. The consistent reductions in energy per bit across MIMO detection, LDPC, and Polar decoding modules, together with system-wide efficiency improvements through adaptive DVFS and in-memory computing, affirm that energy-efficient design methodologies are both feasible and necessary for supporting the high-performance demands of 5G and forthcoming 6G networks. These results highlight not only the technical viability of near-threshold computing and fine-grained power gating but also their practical potential in ensuring that future communication infrastructure can operate under stringent power budgets without compromising reliability or user experience. The implications extend to multiple domains, including mobile devices, base stations, IoT endpoints, and edge computing platforms, all of which require scalable solutions that can handle dynamic workloads in energy-constrained environments. Based on these outcomes, several practical recommendations can be proposed. First, VLSI designers should prioritize multi-Vt and power-gating techniques in baseband and modem blocks to minimize leakage power without affecting system performance. Second, adaptive workload-aware DVFS policies should be implemented as standard practice in wireless SoCs to ensure energy proportionality, especially under variable traffic conditions. Third, investment in reconfigurable hardware for error-correction and detection tasks should be emphasized, as these blocks represent major energy hotspots in wireless transceivers. Fourth, incorporating in-memory or near-memory computing techniques in arithmetic-intensive modules can provide substantial savings in data-movement energy, which often dominates total consumption in nanoscale designs. Fifth, collaboration between hardware and algorithm designers should be strengthened to ensure that coding schemes, modulation techniques, and detection algorithms are optimized for hardware efficiency as well as theoretical performance. Lastly, industry adoption of hybrid simulation-prototype validation workflows should be encouraged to accelerate the translation of low-power techniques from academic research to commercial systems. In essence, the convergence of power-efficient circuit innovations, flexible architecture-level optimizations, and intelligent system-level control forms a comprehensive design paradigm capable of meeting the dual challenges of energy efficiency and high-performance operation in next-generation wireless communication. By embedding these practices into mainstream design methodologies, the semiconductor and communication industries can ensure the sustainable evolution of wireless infrastructure, delivering faster, more reliable, and greener networks to meet the needs of an increasingly connected world.

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