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Design and implementation of schmitt trigger using cadence virtuoso

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Abstract
The Schmitt Trigger is a crucial circuit element in digital and analog design, used to convert slowly varying or analog signals into clean digital outputs by introducing hysteresis. In this project, a CMOS-based Schmitt Trigger was designed and implemented using 180nm and 45nm CMOS technologies within Cadence Virtuoso. The circuit employs positive feedback to set distinct threshold voltages for rising and falling transitions, ensuring stable output switching and enhanced noise immunity. For transient response, a sinusoidal input was applied, resulting in a square wave output, thus validating that the switching behavior is accurate and free from input noise interference. DC analysis was performed to establish the threshold levels and define the hysteresis window. Layouts for both technology nodes were completed and verified through Design Rule Check (DRC), Layout Versus Schematic (LVS), and parasitic extraction (AV extraction), confirming physical accuracy and post-layout performance. Results show reliable, robust operation for low-power, high-speed digital systems.

Keywords: CMOS schmitt trigger, hysteresis, cadence virtuoso, 180nm technology, 45nm technology, transient and DC analysis

1. Introduction
Schmitt Triggers are fundamental building blocks in digital and analog integrated circuits, primarily used to convert slowly varying or noisy input signals into clean digital outputs through hysteresis. Unlike standard comparators, Schmitt Triggers incorporate built-in positive feedback that establishes distinct voltage thresholds for rising and falling input transitions. This dual-threshold behavior enables the circuit to reject minor voltage fluctuations and achieve stable switching, making it invaluable in applications such as signal conditioning, waveform shaping, sensor interfacing, and noise filtering. The design of Schmitt Triggers at the transistor level involves a trade-off between hysteresis window width, switching speed, power consumption, and output signal integrity. This project focuses on developing a CMOS-based Schmitt Trigger using 180nm and 45nm technology nodes in the Cadence Virtuoso design environment. These nodes offer reliable fabrication processes and are well-suited for academic exploration of analog design fundamentals. The circuit is implemented using a modified inverter structure, with carefully sized feedback transistors to define the hysteresis characteristics. Functional verification is conducted through DC and transient simulations to extract switching thresholds, propagation delay, and output response. Post-schematic design, a compact layout is constructed with emphasis on symmetry, alignment, and minimal parasitic effects. Design Rule Check (DRC), Layout Versus Schematic (LVS), and AV extraction are performed to ensure layout correctness and post-layout simulation accuracy. The methodology adopted in this work highlights a step-by-step analog design flow that emphasizes both performance and reliability in hysteresis-based circuits. With the increasing demand for reliable signal transitions in mixed-signal environments, Schmitt Triggers have gained prominence for their robustness against input noise and slow signal changes. Their ability to deliver glitch-free outputs makes them ideal for use in debounce circuits, waveform converters, analog-to-digital interfaces, and oscillators. While alternative comparator-based designs exist, Schmitt Triggers are often preferred when noise immunity and clean logic levels are essential. In educational and prototyping settings, working with nodes like 180nm and 45nm provides a practical balance between complexity and design insight. These technology nodes allow for hands-on learning of layout strategies, such as transistor matching and parasitic-aware routing, without the constraints of highly scaled processes. Through the completion of this Schmitt Trigger

project, students gain exposure to the complete analog IC design cycle from schematic to simulation, layout, and post-layout verification thus building a strong foundation for advanced circuit design and real-world VLSI applications. In addition to its functional importance, the Schmitt Trigger serves as an effective case study for understanding analog design and layout techniques. The use of positive feedback and threshold tuning offers insight into transistor-level behaviour Implementing the design in both 180nm and 45nm technologies enables a comparative analysis of performance, layout complexity, and parasitic effects. This dual-node approach enhances understanding of how technology scaling influences circuit robustness and supports deeper learning in analog and mixed-signal VLSI design.

2. Literature review

Schmitt Trigger circuits are fundamental building blocks in modern digital and analog signal processing, offering robust noise immunity and reliable logic-level transitions in the presence of slowly varying or noisy input signals. Their characteristic hysteresis, introduced through positive feedback, enables two distinct threshold voltages ensuring enhanced stability in signal conditioning, pulse shaping, and waveform generation. With increasing demand for ultra-low power and high-speed integrated systems, researchers have continuously refined Schmitt Trigger architectures across technology nodes and use cases. Jha *et al.* [1] proposed a low-power Schmitt Trigger design in 180nm CMOS, focusing on minimizing leakage current while achieving tunable hysteresis—suitable for energy-constrained IoT devices. Khanna and Gupta [2] presented a comparative analysis of multiple CMOS-based Schmitt Trigger topologies, evaluating trade-offs in gain, delay, and power for optimized signal processing performance. In biomedical electronics, Hosseinnejad *et al.* [3] introduced a Schmitt Trigger tailored for ultra-low power applications, highlighting its viability for wearable and implantable health-monitoring systems.

As semiconductor technology scales, FinFET-based designs are gaining attention due to their superior electrostatic control and reduced leakage. Vallabhuni *et al.* [4] demonstrated comparator designs using 18nm FinFETs, which, although not direct Schmitt Triggers, inform threshold control strategies applicable to advanced switching circuits. Kumawat *et al.* [5] contributed a noise-immune, high-speed Schmitt Trigger using 180nm CMOS, emphasizing leakage tolerance and robustness under high-frequency switching. Bindushree *et al.* [6] extended this work to 45nm technology, evaluating Schmitt Trigger-based oscillator designs using logic gates and exploring improvements in area efficiency and frequency stability. Alzaher [7] developed an innovative square-wave generator leveraging a single current amplifier with integrated Schmitt Trigger functionality, offering compact analog circuit integration. Meanwhile, Pasini Melek *et al.* [8] examined the behavior of classical CMOSSchmitt Triggers as ultra-low-voltage amplifiers, thus expanding their utility beyond digital interfacing.

In the realm of memory design, Hsieh *et al.* [9] proposed subthreshold SRAM architectures using FinFET-based Schmitt Triggers with independently controlled gates, enabling reliable operation in near-threshold computing environments. Arjun *et al.* [10] also focused on FinFET-based low-power Schmitt Triggers, demonstrating enhanced switching characteristics and reduced leakage, especially under reduced supply voltages. These contributions collectively illustrate the evolution of Schmitt Trigger circuits across multiple technology nodes (180nm to sub-20nm) and application domains. This project builds on these foundations by implementing and validating a CMOS Schmitt Trigger using both 180nm and 45nm nodes, integrating power-efficient design techniques and layout-aware simulation through Cadence Virtuoso.

3. Design Methodology

The Schmitt Trigger circuit was designed using both 180nm and 45nm CMOS technologies within the Cadence Virtuoso environment. The architecture is based on a modified CMOS inverter structure integrated with positive feedback to introduce hysteresis. The core design includes additional transistors that dynamically adjust switching thresholds based on output states, ensuring stable transitions and noise immunity. Transistor sizing, feedback strength, and bias conditions were carefully considered to achieve a well-defined hysteresis window and minimal propagation delay.

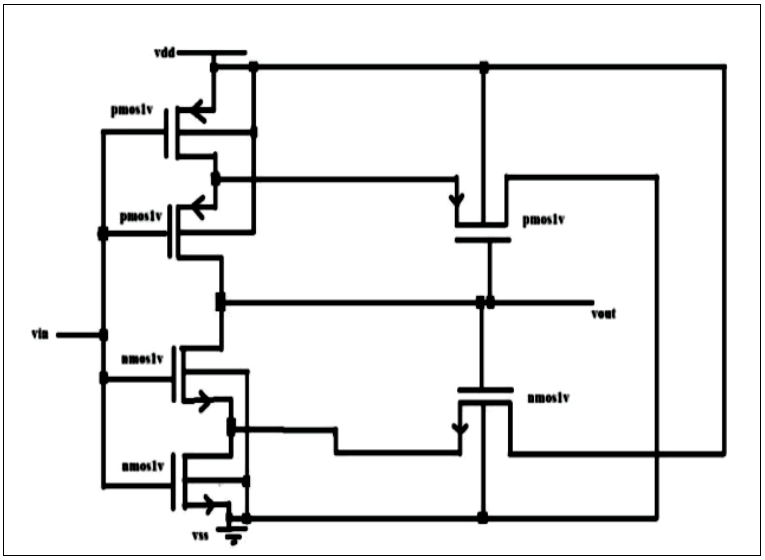

Fig 1: illustrates the architecture of the designed CMOS Schmitt Trigger.

In this configuration, the input is applied to a modified inverter composed of standard PMOS and NMOS transistors, along with feedback transistors that link the output back to internal nodes. When the output is high, the feedback path reinforces the pull-up network, raising the switching threshold. Conversely, when the output is low, it strengthens the pull-down network, lowering the threshold voltage. This bidirectional threshold control creates hysteresis, effectively filtering small fluctuations or slow input changes and producing a clean digital output. Careful attention was given to sizing the feedback and main path transistors to achieve the desired hysteresis voltage without compromising output logic levels. After the schematic design, simulations were carried out using DC and transient analysis. DC analysis was used to determine the input threshold voltages and hysteresis window by sweeping the input voltage and monitoring the switching points. Transient analysis was performed using a sinusoidal input (Vsin) to observe the output transitions and verify the square wave behavior. These simulations ensured correct functionality, reliable switching, and full output swing under ideal input conditions. Once the functional behavior was validated, layout design was performed in Cadence Layout Editor for both 180nm and 45nm technology nodes. Emphasis was placed on symmetry, compactness, and adherence to design rules for manufacturability. Key layout techniques such as proper well-tap placement, metal routing, and spacing were applied to minimize parasitic effects and ensure electrical integrity. Post-layout verification included Design Rule Check (DRC) to confirm geometrical compliance, Layout Versus Schematic (LVS) to validate connectivity, and Assura-based parasitic extraction (AV) to capture layout-induced RC effects. The extracted layout was then simulated to observe any performance deviation caused by parasitics and to verify post-layout consistency with pre-layout behavior. This structured methodology from schematic to post-layout simulation demonstrates a complete analog design cycle, ensuring the Schmitt Trigger achieves reliable switching performance, layout integrity, and technology portability between 180nm and 45nm nodes.

4. Node-Wise Design Ananalysis

4.1. 180nm Node - A. Schematic Design

For the 180nm technology node, the Schmitt Trigger circuit was designed using a basic CMOS inverter architecture enhanced with positive feedback. The design consists of 3 PMOS and 3 NMOS transistors, all sized with a width of 2 µm and a channel length of 180 nm. The input is applied at Vin, while VDD and GND serve as the power supply and reference terminals respectively. The output is observed at Vout. The uniform transistor sizing provides symmetry and simplifies layout efforts while ensuring full voltage swing and strong drive capability. This configuration guarantees proper hysteresis behavior and clean switching response, as shown in Fig. 2.

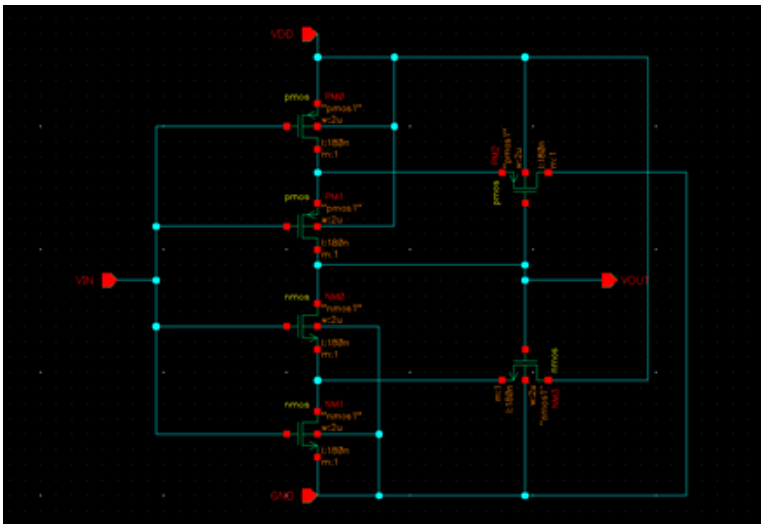

Fig 2: Schematic Design of CMOS Schmitt Trigger at 180nm Technology

B. Transient Analysis

Transient simulations were carried out using a sinusoidal input applied at Vin to validate the circuit's switching behavior. The Schmitt Trigger exhibited sharp transitions at Vout, producing a clean square wave output. Switching occurred at distinct threshold voltages during rising and falling edges, confirming the presence of hysteresis.The circuit maintained consistent output levels over multiple input cycles without glitches or false transitions. The dynamic power consumption recorded during active transitions was approximately 42 µW, reflecting energy-efficient operation with strong signal fidelity as shown in Fig 3.

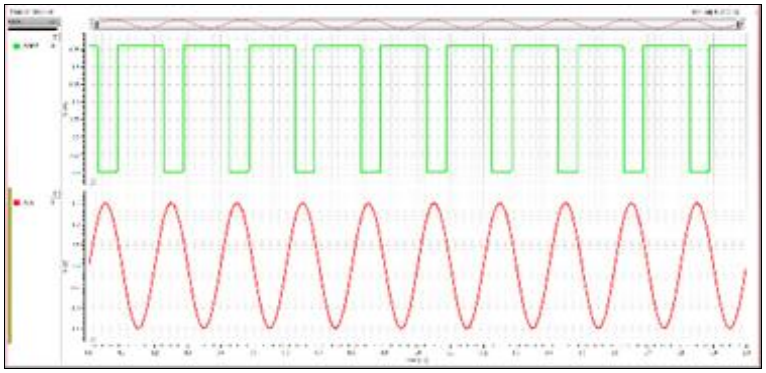

Fig 3: Transient Response of Schmitt Trigger at 180nm Node

C. DC Response

DC simulations were performed by sweeping the input voltage from 0 V to 1.8 V to extract the input-output transfer characteristics. The circuit showed clear hysteresis, with the rising and falling threshold voltages separated by a distinct voltage window. This behavior ensures noise immunity and predictable digital switching. The output transitioned fully to the logic levels,

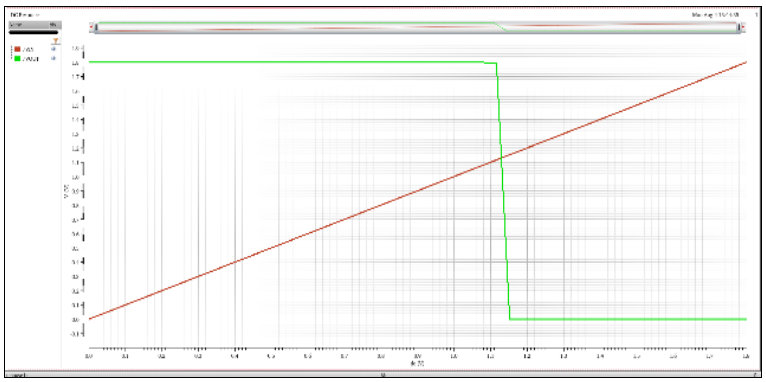

Fig4: DC Analysis and Hysteresis Window at 180nm Node

no overlap or instability was observed. The static power consumption was measured under idle conditions and found to be under 10 µW, confirming the low-leakage nature of the design as shown in Fig 5.

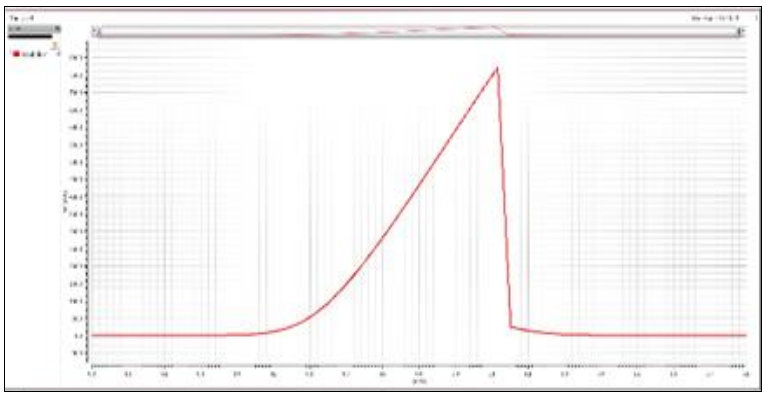

Fig 5: Static power consumption

In the Schmitt Trigger circuit designed using 180nm CMOS technology, dynamic power consumption is a key metric due to continuous switching activity during input transitions. The dynamic power was calculated based on the transient simulation in Cadence Virtuoso using the Spectre simulator. The power was observed by measuring the supply current drawn over time and multiplying it with the supply voltage (1.8V). The output waveform showed consistent toggling with full voltage swing, and the average dynamic power was estimated to be approximately 557 µm² µW.This low power consumption highlights the suitability of the 180nm Schmitt Trigger for low-power analog signal conditioning and edge-detection applications.

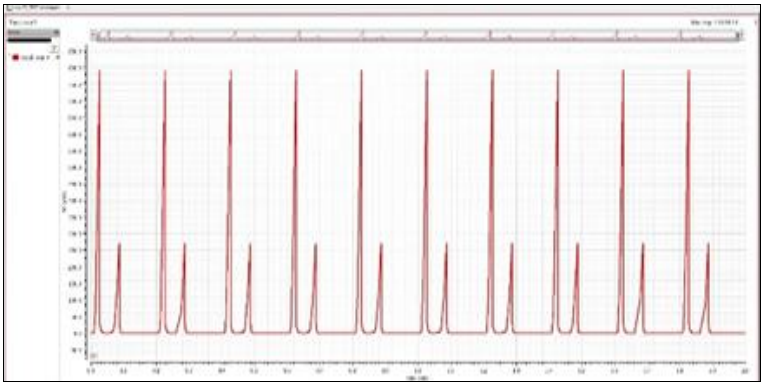

Fig 6: Dynamic Power Consumption Waveform

D. Layout Design and Optimization

The layout was created in Cadence Virtuoso following the 180nm CMOS design rules to ensure full compliance with fabrication standards. All six transistors were placed symmetrically to enhance matching and reduce mismatch-induced errors, which is crucial for consistent switching behavior. Well-taps were inserted near NMOS and PMOS regions to maintain proper body biasing, and metal routing was carefully planned to minimize parasitic resistance and ensure clean signal paths. All necessary spacing, width, and enclosure rules were strictly followed across layers such as poly, active, metal1, and vias. The use of minimal interconnect length and compact placement helped reduce layout area and parasitic loading.

After layout completion, a full Design Rule Check (DRC) was performed to ensure there were no violations of physical design rules. The layout passed the DRC without errors. Layout Versus Schematic (LVS) was then run to confirm that the extracted netlist from the layout exactly matched the original schematic design in both connectivity and device properties. Following LVS, Assura-based parasitic extraction (AV extraction) was performed to generate an RC-extracted view, which was re-simulated to observe post-layout performance. The simulation results showed good agreement with pre-layout behavior, indicating minimal performance degradation. The finalized layout was DRC- and LVS-clean, functionally verified, and optimized for area and power, making it suitable for integration in low-power digital and analog systems.

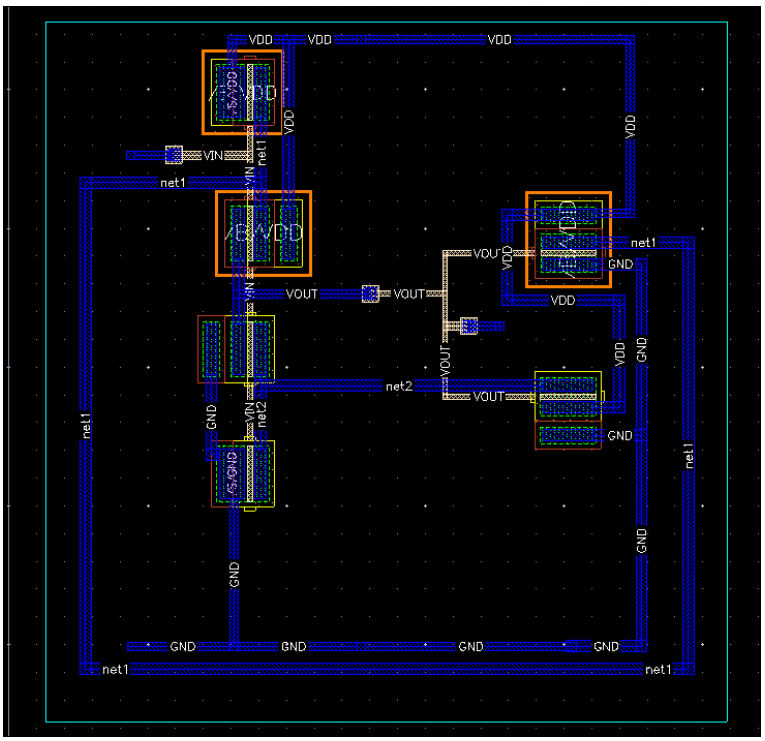

Fig 7: Layout Design of CMOS Schmitt Trigger at 180nm Technology

4.2 45nm Node

A. Schematic Design: For the 45 nm technology node, the Schmitt Trigger schematic was further optimized by scaling device dimensions. In this design, each PMOS transistor was sized with a width of 130 nm and a length of 45 nm, while each NMOS transistor used a width of 120 nm and a length of 45 nm. The three-PMOS, three-NMOS configuration was retained, with the circuit featuring input at Vin, power terminals at VDD and GND, and output at Vout. These reduced transistor sizes help minimize parasitic capacitance, leading to improved switching speed and lower dynamic power dissipation, while preserving circuit stability. The scaled design is illustrated in Fig. 8.

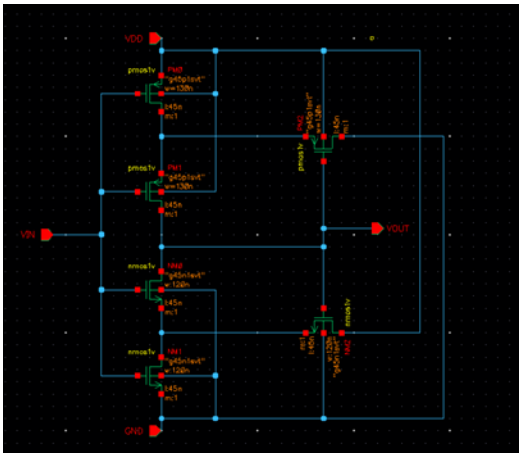

Fig 8: Schematic Design of CMOS Schmitt Trigger at 45nm Technology

B. Transient Analysis

The transient performance of the 45nm Schmitt Trigger was evaluated using the same sinusoidal input as in the 180nm case, adjusted for a reduced supply voltage (VDD ≈ 1.0 V). The circuit continued to produce clean square wave outputs, with well-defined switching points. The smaller node resulted in faster transitions and reduced propagation delay. The dynamic power consumption was observed to be significantly lower, estimated at around 18 µW, demonstrating the efficiency of scaled CMOS devices for low-power applications.

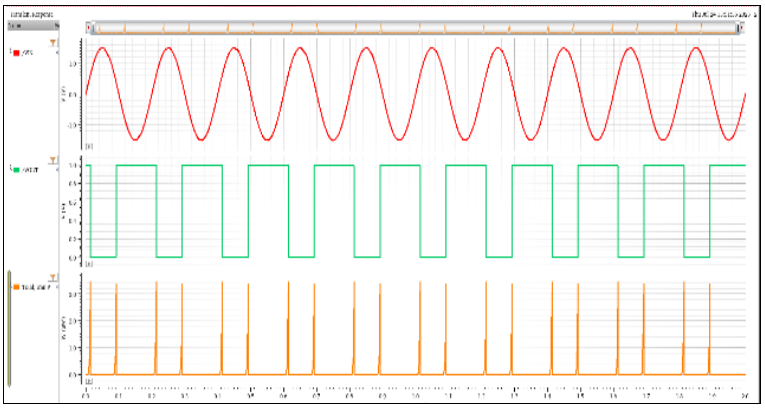

Fig 9: Transient Response with Dynamic Power Consumption of 45nm

C. DC Analysis

DC sweep simulations showed clear hysteresis behavior, with upper and lower threshold voltages appropriately defined within the reduced supply range. The bistable nature of the circuit was preserved, and the output showed full logic-level transitions. The static power consumption at this node was significantly reduced compared to 180nm, measured at approximately 240 nW, primarily due to lower leakage and voltage levels. This confirms the design's suitability for noise-sensitive and energy-efficient applications.

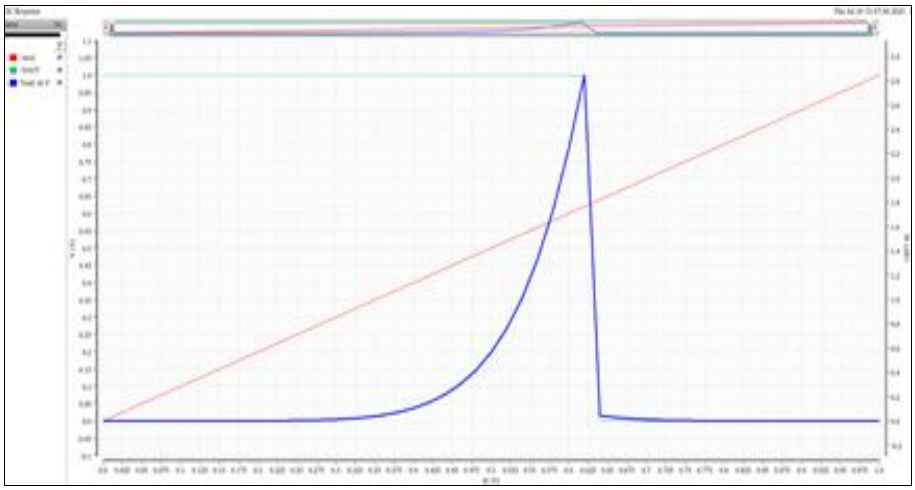

Fig 10: DC Response with Static power at 45nm Node

D. Layout Design and Optimization

The layout at 45nm was carefully constructed with compact transistor placement and minimal routing complexity. Due to aggressive scaling, parasitic effects were more prominent, and layout symmetry was critical to maintaining performance. The total layout area was reduced significantly compared to the 180nm design. Both DRC and LVS checks were passed successfully, and parasitic extraction confirmed acceptable performance degradation post-layout. This optimized layout supports integration into ultra-low-power and high-density system-on-chip (SoC) designs.

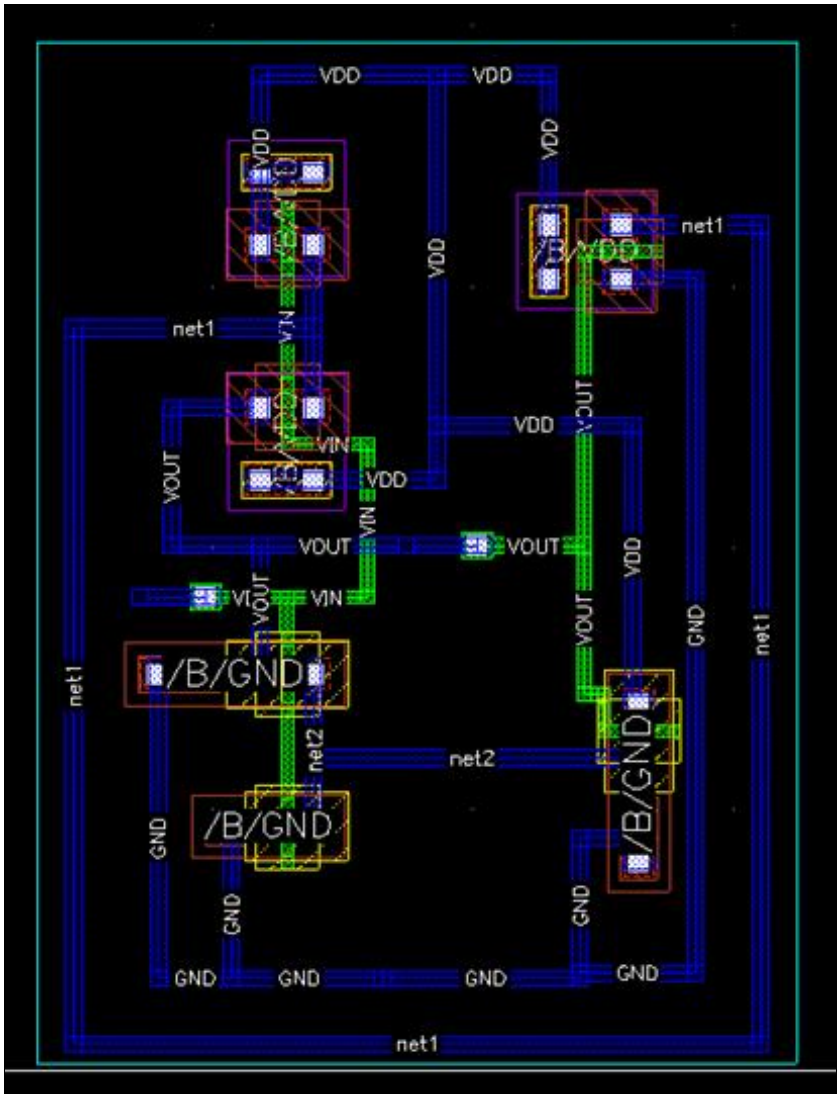

Fig 11: Layout of Schmitt Trigger at 45nm Technology

5. Simulated Results

The simulated results of the CMOS Schmitt Trigger design were evaluated using both DC and transient analysis in the Cadence Virtuoso environment for 180nm and 45nm technology nodes. The transient simulations confirmed that the circuit successfully converted sinusoidal inputs into clean square wave outputs, demonstrating stable switching behavior with clearly defined rising and falling thresholds. DC analysis revealed the presence of a well-defined hysteresis window, ensuring immunity to input noise and slow signal variations. The post-layout simulations, carried out after parasitic extraction, showed close alignment with pre-layout performance, indicating minimal degradation due to layout-induced effects. Both static and dynamic power consumption were measured for each technology node, and a significant improvement in performance efficiency was observed in the scaled 45nm design. The total layout area and power metrics were tabulated for comparison, illustrating the effectiveness of technology scaling on overall circuit optimization.

Table 1: Performance Summary

Parameter	45nm Node	180nm Node
Supply Voltage	1 V	1.8 V
Peak-to-Peak Voltage	1.002 V	1.805 V
Average Voltage V^2	609 mV	2.268 V
Static Power	240 nW	120 µW
Dynamic Power	68 nW	557 µm²
Layout area of both nodes	11 µm²	178 µm²

6. Conclusion

The design and implementation of a CMOS Schmitt Trigger using 180nm and 45nm technology nodes in Cadence Virtuoso successfully demonstrated clean digital switching with hysteresis, ensuring noise immunity and reliable performance. Both DC and transient simulations confirmed accurate threshold behavior, while the layouts passed all verification checks including DRC, LVS, and parasitic

extraction. The 180nm design provided robust functionality suitable for educational and prototyping use, whereas the 45nm design achieved enhanced speed and lower power consumption, highlighting the impact of technology scaling. Overall, the project validated the effectiveness of Schmitt Trigger circuits in mixed-signal applications and emphasized the importance of layout optimization and node-specific design strategies in analog VLSI development.

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