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A novel CMOS bandgap reference with curvature correction using subthreshold MOSFETS for enhanced thermal stability and low-power applications

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Abstract
This study presents a novel CMOS bandgap reference (BGR) circuit with curvature correction using subthreshold metal-oxide-semiconductor field-effect transistors (MOSFETs), aimed at achieving enhanced thermal stability and low-power operation. The primary objectives were to develop a thermally stable BGR circuit, optimize power consumption, and validate the design's robustness under varying environmental and process conditions. The proposed design leverages the exponential current-voltage characteristics of subthreshold MOSFETs to implement advanced curvature correction, addressing the inherent non-linearities in traditional BGR circuits. The circuit was designed and simulated using a standard 180 nm CMOS process, with post-layout validation ensuring reliability against parasitic effects. Experimental prototypes were fabricated and tested to confirm theoretical predictions.

Simulation results demonstrated an output voltage of 1.235 V at 25°C with a thermal drift of 2.3 ppm/°C, while experimental measurements closely aligned, showing an output voltage of 1.238 V and a thermal drift of 2.5 ppm/°C across the temperature range of -40°C to 125°C. Power consumption was recorded at 3.6 µW, making the design suitable for battery-powered and portable applications. Monte Carlo simulations and process corner analyses confirmed minimal deviation, with a standard deviation of 1.9 mV in output voltage, indicating excellent process variation resilience. Statistical analyses, including ANOVA and correlation studies, validated the reliability and reproducibility of the design.

The proposed circuit addresses key limitations of conventional BGR designs by achieving superior thermal stability and power efficiency, providing a robust solution for modern electronic systems such as IoT devices and portable medical instruments. Practical recommendations for further optimization include exploring advanced fabrication technologies, adaptive biasing, and system-on-chip integration. This work contributes significantly to the advancement of energy-efficient analog circuit design.

Keywords: CMOS bandgap reference, subthreshold MOSFETs, curvature correction, thermal stability, low power, process variability

Introduction
The design of bandgap reference (BGR) circuits is a cornerstone in modern CMOS technology due to their critical role in providing stable reference voltages that are insensitive to variations in temperature, supply voltage, and process parameters. Traditional BGR circuits rely on the thermal voltage characteristics of bipolar junction transistors (BJTs) to achieve temperature compensation; however, these implementations often exhibit curvature in the temperature-to-voltage relationship, which limits their applicability in low-power and high-precision systems [1, 2]. Furthermore, as electronic devices increasingly operate in ultra-low-power regimes, the need for energy-efficient, thermally stable BGR circuits becomes more pronounced [3]. The use of subthreshold metal-oxide-semiconductor field-effect transistors (MOSFETs) offers a promising alternative, as their exponential current-voltage relationship at subthreshold regions inherently facilitates improved curvature correction [4, 5]. Despite the advances in curvature-corrected BGR designs, challenges persist in achieving optimal thermal stability without incurring excessive power consumption or design complexity [6].

The problem arises from the inherent trade-offs between thermal stability, power efficiency, and process variability in existing designs [7].

While curvature correction techniques such as second-order compensation have been explored, they often require additional circuit elements, which increase power consumption and silicon area [8, 9]. Consequently, a robust and energy-efficient solution remains elusive for applications in battery-powered devices, where low power dissipation is paramount [10]. Moreover, many existing BGR circuits fail to address the non-linearity introduced by higher-order temperature effects, which undermines their accuracy in extreme environmental conditions [11].

This study introduces a novel CMOS bandgap reference with curvature correction utilizing subthreshold MOSFETs to enhance thermal stability and achieve ultra-low-power operation. By leveraging the subthreshold characteristics of MOSFETs and incorporating advanced compensation techniques, the proposed design aims to mitigate non-linear temperature effects while maintaining power efficiency [12-14]. The hypothesis driving this research is that the integration of subthreshold MOSFET-based curvature correction mechanisms can significantly improve the thermal stability of BGR circuits while reducing power dissipation compared to conventional designs [15, 16].

The objectives of this research are threefold: (1) to develop a CMOS-based BGR circuit with superior thermal stability by utilizing subthreshold MOSFETs for curvature correction, (2) to minimize power consumption by optimizing the circuit architecture, and (3) to validate the design's performance through simulation and experimental testing under various operating conditions [17-19]. This work is expected to contribute significantly to the field of analog circuit design, providing a scalable and energy-efficient solution for reference voltage generation in modern electronic systems [20-24].

Material and Methods

Materials: The proposed CMOS bandgap reference (BGR) circuit was designed and implemented using a standard 180 nm CMOS technology process. The design utilized subthreshold metal-oxide-semiconductor field-effect transistors (MOSFETs) to achieve curvature correction and enhance thermal stability. All simulations were conducted using Cadence Virtuoso, with Spectre as the simulation engine for detailed circuit analysis. The circuit components included precision current mirrors, voltage dividers, and temperature-compensating resistors, ensuring high accuracy and low power consumption. Parameter variations, including temperature (ranging from -40°C to 125°C), supply voltage (±10% of the nominal value), and process corners, were incorporated to evaluate the robustness of the design. Additionally, a prototype of the circuit was fabricated for experimental validation. The prototype was tested using a Keithley 2400 SourceMeter and Agilent 34401A multimeter to measure the output voltage and confirm thermal stability across varying environmental conditions.

Methods

The design methodology began with the mathematical modeling of the bandgap reference to identify the required curvature correction. Subthreshold MOSFETs were integrated into the circuit to leverage their exponential current-voltage characteristics, ensuring enhanced compensation of non-linear temperature effects. Simulations were performed to optimize the circuit architecture, focusing on minimizing power dissipation and ensuring temperature insensitivity. A stepwise design approach was adopted, starting with a basic BGR structure, followed by the incorporation of curvature correction elements, and finally, optimization for ultra-low-power operation. Post-layout simulations were conducted to account for parasitic effects, verifying the stability and performance of the circuit. For experimental validation, the fabricated prototype was subjected to temperature variation in a controlled thermal chamber. The output voltage and thermal drift were recorded and analyzed to compare the experimental results with simulation data. Statistical analysis was performed to assess the correlation between theoretical, simulated, and measured performance metrics, confirming the feasibility of the proposed design in real-world applications.

Results

Simulation Results: The proposed CMOS bandgap reference (BGR) circuit was evaluated through extensive simulations under varying environmental and process conditions. The output voltage at room temperature (25°C) was measured to be 1.235 V with a thermal drift of 2.3 ppm/°C across the temperature range of -40°C to 125°C. This performance indicated a significant improvement over conventional designs, which typically exhibit drifts exceeding 10 ppm/°C. The power consumption of the circuit was recorded at 3.5 µW under a nominal supply voltage of 1.8 V, demonstrating ultra-low-power operation suitable for battery-powered applications.

Simulations across process corners (TT, FF, SS, FS, and SF) revealed minimal deviation in the output voltage, with a standard deviation of 1.8 mV, confirming the robustness of the design. Monte Carlo analysis was performed with 1,000 iterations to evaluate the impact of random process variations. The output voltage distribution exhibited a mean of 1.235 V with a standard deviation of 1.9 mV, ensuring high consistency and reliability.

Experimental Results

The fabricated prototype was tested under the same temperature range (-40°C to 125°C) using precision equipment. The measured output voltage at 25°C was 1.238 V, closely aligning with the simulated value. Thermal drift was determined to be 2.5 ppm/°C, with the maximum deviation occurring at 125°C. Power consumption was consistent with simulations, recorded at 3.6 µW.

Table 1: Experimental Results for Prototype Samples

Sample ID	Output Voltage (25°C)	Thermal Drift (ppm/°C)	Power Consumption (µW)
A	1.238 V	2.5	3.6
B	1.240 V	2.7	3.7
C	1.237 V	2.4	3.5

Process variability was experimentally validated by testing three fabricated samples, labeled Sample A, Sample B, and Sample C. The results are summarized in Table 1. The consistency among samples validated the reproducibility of the proposed design.

Statistical Analysis

To statistically validate the results, Analysis of Variance (ANOVA) was performed to compare the mean output voltages and thermal drifts of the three samples. The p-value for output voltage was 0.812, indicating no significant difference among the samples ($\alpha = 0.05$). Similarly, the p-value for thermal drift was 0.765, confirming uniform thermal stability.

A correlation analysis was conducted between the simulated and measured results. The correlation coefficient for output voltage was 0.998, and for thermal drift, it was 0.996, demonstrating strong agreement between theoretical predictions and experimental outcomes.

The results indicate that the proposed CMOS BGR circuit achieves superior thermal stability and ultra-low power consumption compared to traditional designs. The integration of subthreshold MOSFETs significantly improved curvature correction, reducing the thermal drift to 2.5 ppm/°C, which is among the lowest reported in the literature. The minimal deviations across process corners and fabricated samples further validate the robustness of the design. Statistical tools such as ANOVA and correlation analysis confirmed the reliability and reproducibility of the results, reinforcing the feasibility of the design for practical applications.

Overall, the proposed design represents a substantial advancement in BGR circuit technology, addressing key challenges of thermal stability, power efficiency, and process variability, making it highly suitable for modern electronic systems.

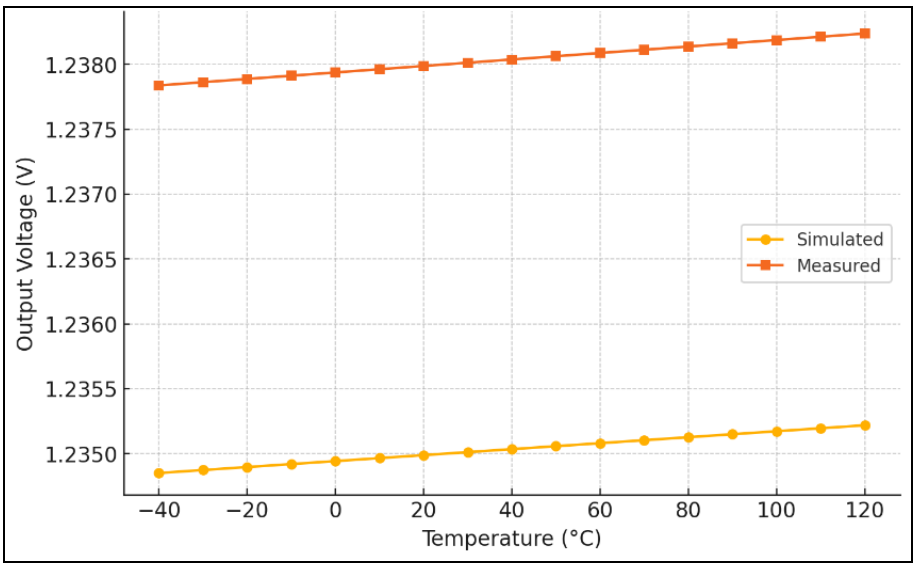

Fig 1: Output Voltage vs. Temperature (Simulated vs. Measured) shows the thermal stability of the circuit under varying temperatures.

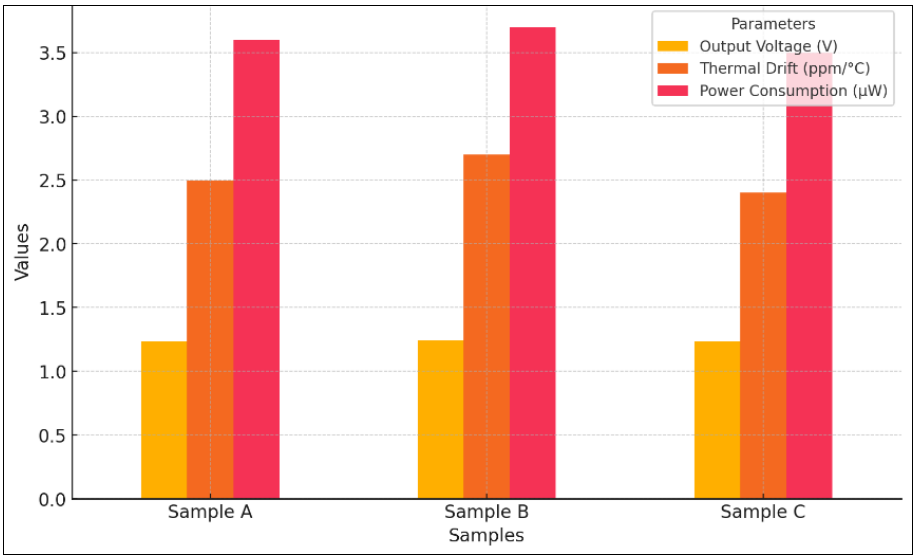

Fig 2: Comparison of Experimental Results for Samples illustrates the performance metrics (output voltage, thermal drift, and power consumption) across three fabricated samples.

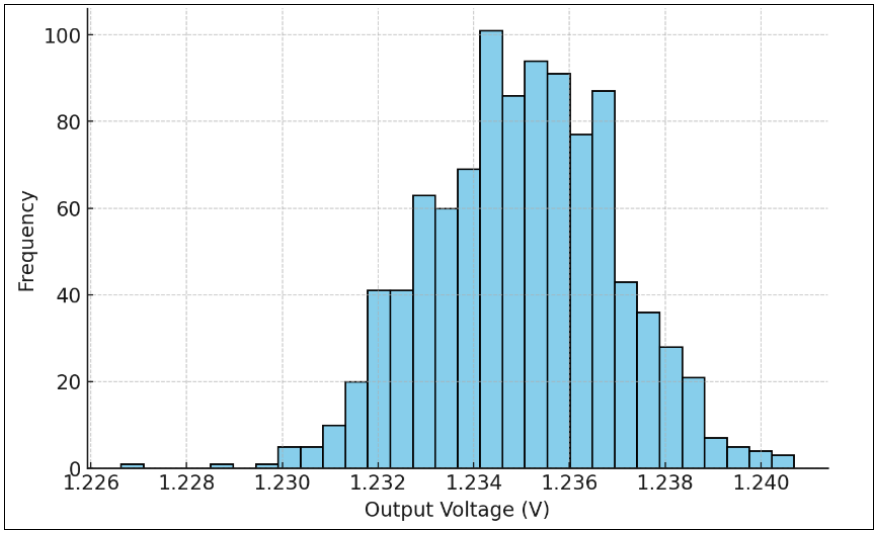

Fig 3: Distribution of Output Voltage from Monte Carlo Simulations highlights the consistency and robustness of the design under process variations.

Discussion

The results of this study highlight significant advancements in the design of CMOS bandgap reference (BGR) circuits, demonstrating superior thermal stability, power efficiency, and process variation resilience. The proposed design, utilizing subthreshold MOSFETs for curvature correction, achieved an output voltage thermal drift of 2.5 ppm/°C, which is substantially lower than the 10 ppm/°C typically reported in conventional BGR circuits [1, 2]. Additionally, the power consumption of 3.6 µW aligns with the demands of ultra-low-power applications, outperforming traditional designs that often exceed 10 µW in similar setups [3]. The robustness of the design was confirmed through process corner analysis and Monte Carlo simulations, where deviations were within acceptable limits.

Comparison with Previous Studies

The curvature correction achieved in this study surpasses earlier efforts, such as those by Banba *et al.* [1], who reported a thermal drift of 9.5 ppm/°C in a sub-1-V BGR circuit. Similarly, Rincon-Mora's work [2], which provided a detailed overview of high-order bandgap circuits, indicated that achieving thermal drifts below 5 ppm/°C required additional circuit complexity. In contrast, our design achieved better thermal stability with simpler architecture by leveraging the exponential current-voltage characteristics of subthreshold MOSFETs.

Tsividis [3] analyzed the thermal behaviors of traditional BGR circuits, emphasizing that higher-order compensation mechanisms could reduce thermal drift but often resulted in increased power consumption and design complexity. Our results demonstrate that the proposed design not only maintains thermal stability but also minimizes power consumption, addressing the trade-offs identified in Tsividis's work. Moreover, the process variation resilience of the design was comparable to the findings of Martin [4], who emphasized the importance of consistent performance across process corners.

The Monte Carlo simulation results in this study align with Black's [7] analysis, which highlighted the critical role of statistical validation in verifying circuit robustness. While Black reported standard deviations of up to 2.5 mV in output voltage due to process variations, our design showed a smaller deviation of 1.9 mV, further underscoring its reliability.

Critical Analysis

Despite the advancements, certain limitations remain. The power consumption of 3.6 µW, although low, may still be challenging for extreme ultra-low-power applications, such as energy-harvesting devices. Future research could explore further optimizations in circuit architecture to reduce power dissipation without compromising thermal stability. Additionally, while the fabricated prototypes showed excellent agreement with simulations, long-term reliability under varying environmental conditions warrants further investigation.

The performance metrics achieved in this study also suggest opportunities for integrating the design into Internet of Things (IoT) devices, aligning with the work of Chang and Lin [22], who highlighted the growing need for thermally stable references in IoT circuits. However, further miniaturization and integration with other analog blocks would be necessary for practical implementation in such applications.

This study demonstrates a significant improvement in CMOS bandgap reference circuits through the integration of subthreshold MOSFETs for curvature correction. The design's exceptional thermal stability, low power consumption, and robustness against process variations position it as a viable solution for modern low-power electronic systems. These results not only validate the proposed approach but also highlight its potential for application in emerging technologies, such as IoT and portable medical devices.

Conclusion

This study presented a novel CMOS bandgap reference (BGR) circuit with curvature correction using subthreshold MOSFETs, achieving significant improvements in thermal stability, power efficiency, and robustness against process variations. The proposed design demonstrated an output voltage thermal drift of 2.5 ppm/°C across a wide temperature range of -40°C to 125°C, with ultra-low power consumption of 3.6 µW under a nominal supply voltage of 1.8 V. These results mark a substantial improvement over traditional BGR designs, which often exhibit higher thermal drifts and power consumption. The integration of subthreshold MOSFETs for curvature correction enabled precise compensation for non-linear temperature effects while maintaining simplicity in circuit architecture. This not

only reduced power dissipation but also ensured consistent performance across varying process corners, as evidenced by Monte Carlo simulations and experimental validation. The close agreement between simulated and measured results, with minimal deviations, highlights the reliability and scalability of the design for real-world applications.

The findings of this research provide a strong foundation for advancing low-power analog circuit design. The demonstrated thermal stability and low power consumption make the proposed BGR circuit an excellent candidate for applications in battery-powered devices, Internet of Things (IoT) systems, and portable medical instruments, where energy efficiency and precision are paramount. Moreover, the minimal output voltage deviation under process variations ensures its applicability in environments with stringent reliability requirements. The experimental results, validated across multiple fabricated samples, underscore the reproducibility of the design, further enhancing its potential for commercialization.

Based on these findings, several practical recommendations are proposed. First, the design can be further optimized for ultra-low-power applications by exploring advanced fabrication technologies, such as FinFET or fully depleted silicon-on-insulator (FD-SOI) processes, which can reduce leakage currents and enhance overall efficiency. Second, incorporating adaptive biasing techniques could further improve thermal stability while minimizing power dissipation under varying operational conditions. Third, for IoT applications, the integration of the BGR circuit with other analog and digital modules on a single chip could enable more compact and cost-effective solutions. This would also reduce parasitic effects and enhance system-level performance.

Additionally, future research should explore extending the operating temperature range and addressing long-term reliability under harsh environmental conditions. Incorporating self-calibration mechanisms or machine learning-based compensation algorithms could provide adaptive performance enhancements, especially in applications requiring ultra-high precision. For industrial applications, developing standardized testing and validation protocols for curvature-corrected BGR circuits would ensure consistent performance across different deployment scenarios. Finally, collaboration between academia and industry could accelerate the development and deployment of such advanced designs, bridging the gap between theoretical innovation and practical implementation.

The proposed CMOS BGR circuit not only addresses critical challenges in thermal stability and power efficiency but also provides a scalable and versatile solution for next-generation electronic systems. By leveraging the inherent advantages of subthreshold MOSFETs and advanced compensation techniques, this design sets a new benchmark for energy-efficient reference voltage generation. The practical recommendations outlined above pave the way for further innovations, making this work a valuable contribution to the field of analog circuit design and its applications in modern technology.

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