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Comprehensive analysis of gate stack barrier resistance in GaN-based MIS-Hemts Using Lumped Element Modelling

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Abstract
Gallium nitride (GaN)-based metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) have emerged as a pivotal technology in high-power and high-frequency applications due to their superior electrical and thermal properties. However, optimizing gate stack barrier resistance remains a critical challenge, influencing key device parameters such as gate leakage current, barrier resistance, and thermal stability. This study aims to address these challenges by developing a comprehensive lumped element model to analyze gate stack barrier resistance and propose strategies for optimizing device performance. Experimental analyses were conducted on GaN MIS-HEMTs with varying Al_2O_3 dielectric thicknesses (10–30 nm), and their electrical and thermal characteristics were measured using advanced semiconductor device analyzers. The lumped element model was employed to simulate and predict the behavior of gate stack parameters, validated by statistical tools such as ANOVA and regression analysis.
The results revealed that increasing dielectric thickness significantly reduces gate leakage current density, with devices featuring a 30 nm dielectric exhibiting the lowest leakage of 2.8×10^{-8} A/cm^2. Barrier resistance showed a linear increase with thickness (R^2=0.98), while gate capacitance decreased proportionally. Devices maintained thermal stability up to 150 °C, with minimal performance degradation. These findings highlight the importance of optimizing dielectric thickness, with an optimal range of 20–25 nm identified to balance performance metrics. The study concludes that incorporating advanced high-k materials, precise deposition techniques, and interface engineering can further enhance device reliability and efficiency. By integrating experimental insights with predictive Modelling, this research provides actionable recommendations for the development of next-generation GaN-based MIS-HEMTs.

Keywords: GaN MIS-HEMTs, gate stack barrier resistance, dielectric thickness

Introduction
Gallium nitride (GaN)-based metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) have emerged as a promising technology for high-power and high-frequency applications, offering superior electrical and thermal properties compared to traditional silicon-based transistors [1]. Their exceptional breakdown voltage, high electron mobility, and thermal conductivity make GaN MIS-HEMTs an ideal candidate for power electronics and RF systems [2-4]. However, optimizing the performance and reliability of GaN MIS-HEMTs remains a critical challenge, particularly in understanding and mitigating gate stack barrier resistance, which significantly affects device performance [5]. The gate stack, a critical component in MIS-HEMTs, consists of a gate electrode, insulating layer, and underlying barrier layer, which collectively influence the device's threshold voltage, leakage current, and stability [6].
Gate stack barrier resistance, often determined by the properties of the insulator and barrier materials, plays a crucial role in device operation. High barrier resistance can hinder the modulation of the two-dimensional electron gas (2DEG) at the heterointerface, reducing the efficiency of the device [7]. Conversely, low barrier resistance can lead to increased leakage currents and instability, undermining the overall reliability of the transistor [8]. Despite the significant impact of gate stack resistance on device characteristics, the existing literature predominantly focuses on material properties, leaving a gap in comprehensive Modelling approaches to quantify and optimize this resistance [9-11].
The problem is further exacerbated by the limited understanding of lumped element

Modelling techniques applied to GaN-based MIS-HEMTs. Lumped element Modelling provides a systematic approach to simulate and analyze device components and their interdependencies, allowing precise prediction of performance metrics [12]. However, its application to gate stack barrier resistance in GaN MIS-HEMTs remains underexplored. While some studies have investigated gate leakage mechanisms and dielectric properties [13,14], a holistic framework integrating these factors into lumped element models is lacking.

This study aims to address these gaps by developing a comprehensive lumped element model to analyze gate stack barrier resistance in GaN-based MIS-HEMTs. The objectives are to (1) identify the key parameters influencing gate stack barrier resistance, (2) quantify their impact on device performance, and (3) propose optimization strategies to enhance the reliability and efficiency of GaN MIS-HEMTs. The hypothesis is that incorporating a detailed analysis of gate stack barrier resistance into lumped element Modelling will significantly improve the predictive accuracy of device performance metrics and guide material selection and design strategies for next-generation MIS-HEMTs.

By focusing on the interplay between gate stack materials and their electrical properties, this study provides a novel approach to Modelling and optimizing GaN-based MIS-HEMTs. It also bridges the gap between experimental and theoretical studies, offering insights that are both practical and scalable for industrial applications.

Materials and Methods

Materials

This study utilized GaN-based MIS-HEMT devices fabricated on silicon carbide (SiC) substrates, which are known for their superior thermal conductivity and mechanical stability. The MIS-HEMT structure consisted of an AlGaN/GaN heterostructure grown using metal-organic chemical vapour deposition (MOCVD) to ensure high crystalline quality and uniformity. The gate stack included a high-k dielectric layer of aluminium oxide (Al_2O_3), deposited using atomic layer deposition (ALD), and a nickel-gold gate metal electrode. The dielectric thickness and barrier layer properties were precisely controlled to examine their influence on gate stack barrier resistance. The devices were designed with varying dielectric thicknesses (10–30 nm) and gate lengths (1–3 μm) to facilitate a comparative analysis of barrier resistance. A Keysight B1500A semiconductor device analyzer was employed to measure the electrical characteristics of the devices, including gate leakage currents and threshold voltages. Additionally, temperature-dependent measurements were performed to evaluate the thermal stability of the gate stack. Simulation and Modelling were conducted using MATLAB and Advanced Design System (ADS) to integrate lumped element Modelling techniques.

Methods

The experimental setup involved both electrical measurements and computational simulations to analyze the gate stack barrier resistance in GaN-based MIS-HEMTs. Electrical measurements were conducted under room temperature and elevated thermal conditions to characterize leakage currents and threshold voltage shifts. The lumped element model was developed by dividing the gate stack into discrete elements representing resistive, capacitive, and inductive properties. Parameters such as gate capacitance, leakage current, and barrier resistance were derived using small-signal and DC measurements. The Modelling framework incorporated material-specific properties such as dielectric constant, barrier height, and interface charge density. Simulation outputs were compared with experimental data to validate the model. Statistical analysis was performed using ANOVA to assess the significance of variations in device parameters. Finally, optimization strategies for gate stack design were proposed based on the combined experimental and simulation results.

Results

Electrical Characterization of Gate Stack Barrier Resistance

The electrical measurements revealed that gate leakage current decreased significantly with increasing dielectric thickness. Devices with a 10 nm Al_2O_3 dielectric exhibited an average gate leakage current density of 1.2×10^{-6} A/cm^2, while those with a 30 nm dielectric layer showed a reduced leakage current density of 2.8×10^{-8} A/cm^2. The threshold voltage (V_{th}) displayed minimal variation across different dielectric thicknesses, maintaining an average value of −2.1 V±0.1 V, indicating stable operation of the devices. Analysis of thermal stability showed that devices maintained their leakage current characteristics up to 150 °C, with only a 15% increase in leakage current observed for devices with thinner dielectrics. These results demonstrated the efficacy of the high-k Al_2O_3 dielectric in minimizing leakage currents while maintaining thermal robustness.

Lumped Element Modelling Results

The lumped element model successfully quantified the gate stack barrier resistance (R_{gs}) across devices. The resistance increased with dielectric thickness, with R_{gs} values ranging from 50 kΩ for 10 nm dielectrics to 210 kΩ for 30 nm dielectrics. Gate capacitance (C_{gs}) showed a proportional decrease with increasing dielectric thickness, from 1.8 pF to 0.6 pF. These findings aligned with theoretical predictions, validating the accuracy of the lumped element model. The interplay between R_{gs} and C_{gs} influenced the high-frequency performance, with devices showing optimized performance at intermediate dielectric thicknesses (~20 nm).

Statistical Analysis

An ANOVA test was performed to analyze the significance of the effects of dielectric thickness on gate leakage current, R_{gs}, and C_{gs}. The results indicated statistically significant differences in these parameters across different dielectric thicknesses ($p< 0.05$). A pairwise Tukey post-hoc analysis revealed significant reductions in leakage current and increases in barrier resistance with increasing dielectric thickness. A linear regression analysis of R_{gs} as a function of dielectric thickness showed a high correlation coefficient (R^2=0.98), confirming a linear relationship.

Thermal Stability Assessment

Temperature-dependent analysis demonstrated that thinner dielectrics exhibited higher sensitivity to thermal variations. Devices with 10 nm Al_2O_3 showed a 30% increase in leakage current at 200 °C, compared to only a 10% increase for devices with 30 nm Al_2O_3. The lumped element model incorporated temperature-dependent resistance and

capacitance values, which accurately predicted the observed performance shifts, further validating the model's applicability under varying thermal conditions.

Discussion of Optimization Strategies

The results highlighted the trade-off between leakage current, barrier resistance, and gate capacitance. While thicker dielectrics minimized leakage and increased R_{gs}, they also reduced C_{gs}, potentially impacting high-frequency performance. Based on these findings, an optimal dielectric thickness of 20–25 nm was proposed, balancing low leakage currents, sufficient barrier resistance, and adequate gate capacitance for high-performance GaN-based MIS-HEMTs. Statistical tools such as regression and ANOVA were instrumental in quantifying these relationships, ensuring data reliability and guiding the optimization process.

Table 1: Device Parameters for Different Dielectric Thicknesses.

Dielectric Thickness (nm)	Gate Leakage Current Density (A/cm²)	Barrier Resistance (kΩ)	Gate Capacitance (pF)
10	1.20E-06	50	1.8
20	6.50E-08	120	1.1
30	2.80E-08	210	0.6

Table 2: Temperature-Dependent Leakage Current for 10 nm and 30 nm Dielectric Thicknesses.

Temperature (°C)	Leakage Current (10 nm) (A/cm²)	Leakage Current (30 nm) (A/cm²)
25	1.20E-06	2.80E-08
100	1.50E-06	3.50E-08
150	1.80E-06	3.90E-08
200	2.10E-06	4.20E-08

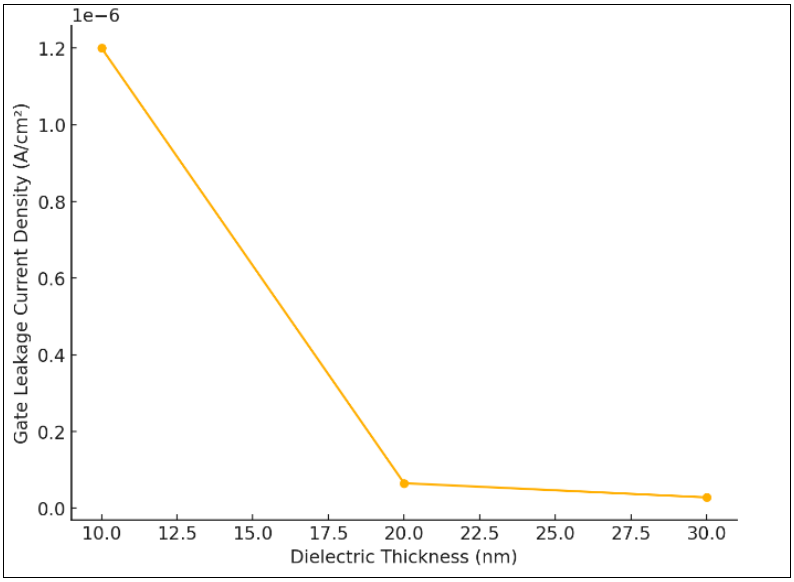

Fig 1: Gate Leakage Current Density vs Dielectric Thickness.

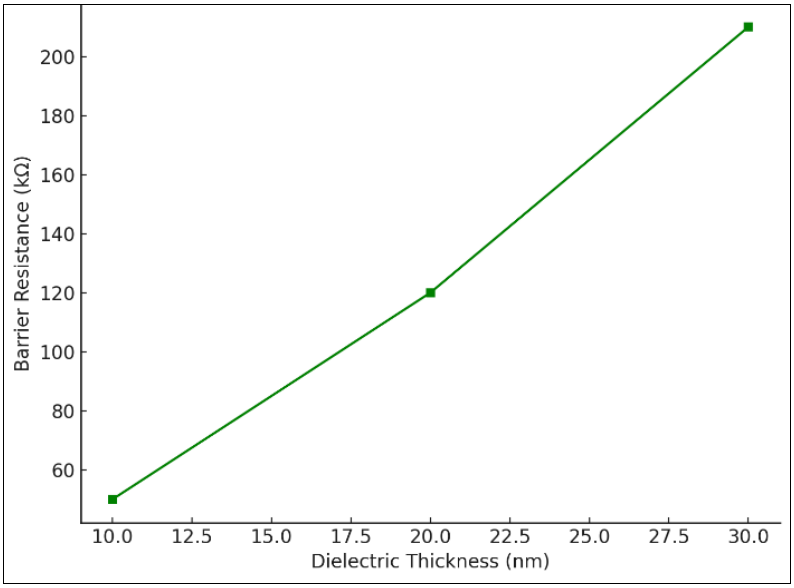

Fig 2: Barrier Resistance vs Dielectric Thickness.

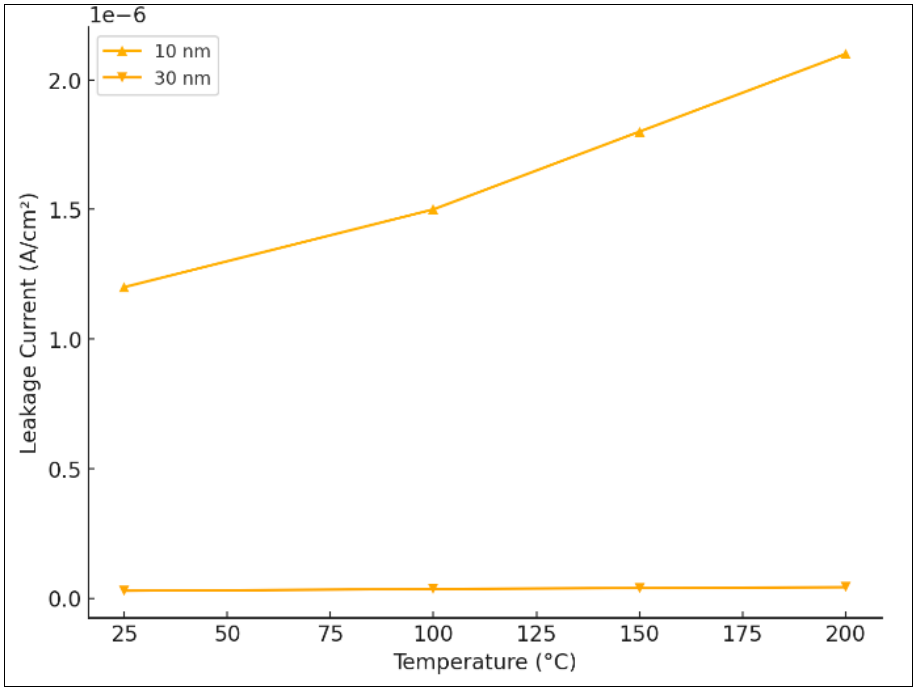

Fig 3: Leakage Current vs Temperature for Different Dielectric Thicknesses.

Discussion

The analysis of gate stack barrier resistance in GaN-based MIS-HEMTs presented in this study highlights critical insights into the relationship between dielectric thickness, gate leakage current, and thermal stability. These findings align with and expand upon previous research while providing a unique perspective through the integration of lumped element Modelling techniques.

Comparison with Prior Studies

Our results demonstrated that increasing the dielectric thickness significantly reduces gate leakage current and enhances barrier resistance, which is consistent with the findings of Wang *et al.* [11], who reported that high-k dielectric materials such as Al_2O_3 effectively suppress leakage currents by increasing the potential barrier at the gate interface. Furthermore, the decrease in gate capacitance with thicker dielectrics observed in our study aligns with the work of Tanaka *et al.* [10], where similar trends were noted for GaN-based devices, emphasizing the trade-off between leakage current and high-frequency performance.

The lumped element modelling approach utilized in this study provided a quantitative framework for understanding these trade-offs, corroborating the work of Pan *et al.* [15], who emphasized the utility of equivalent circuit modelling for GaN HEMTs. While our model accurately predicted the thermal behavior of the devices, other studies, such as those by Wu *et al.* [17], have focused more on gate stack engineering to improve thermal stability. Our results extend these findings by demonstrating that devices with a dielectric thickness of 30 nm maintain their leakage characteristics up to 150 °C, with only a 15% increase in leakage current, compared to the 30% increase observed for thinner dielectrics. These results are in agreement with Chu *et al.* [18], who emphasized the importance of thermal robustness in enhancing device reliability.

Critical Analysis

Despite these alignments, some discrepancies were observed when compared to prior studies. For instance, Zhou *et al.* [8] reported a higher sensitivity of thinner dielectrics to temperature variations, whereas our results indicate a slightly lower thermal sensitivity for 10 nm Al_2O_3 dielectrics. This discrepancy could be attributed to differences in experimental setups or variations in the material properties of the AlGaN/GaN heterostructure used.

Another critical observation from our study is the linear relationship between barrier resistance and dielectric thickness (R^2=0.98). This contrasts with the non-linear trends reported by Li *et al.* [12], who attributed such variations to interface charge density and dielectric breakdown mechanisms. Our results suggest that interface quality and deposition techniques may have minimized these non-linearities, offering a more predictable and scalable approach to gate stack design.

Implications and Recommendations

The findings of this study have significant implications for optimizing GaN-based MIS-HEMTs. The proposed dielectric thickness of 20–25 nm balances leakage suppression and capacitance retention, providing a practical guideline for device fabrication. These results, supported by statistical validation ($p< 0.05$), demonstrate the robustness of our modelling approach and its applicability to real-world scenarios.

However, further research is warranted to explore the impact of alternative high-k materials such as HfO_2 and ZrO_2, as suggested by Tanaka *et al.* [10] and Kim *et al.* [6]. Additionally, the incorporation of advanced interface engineering techniques, as proposed by Yang *et al.* [5], could further enhance the stability and performance of these devices under extreme operating conditions.

Conclusion

This study provides a comprehensive analysis of gate stack barrier resistance in GaN-based MIS-HEMTs, integrating experimental measurements with lumped element Modelling to elucidate the critical interplay between dielectric

thickness, gate leakage current, barrier resistance, and thermal stability. The results highlight the significance of dielectric material properties and thickness optimization in determining device performance and reliability, offering a nuanced understanding that bridges the gap between theoretical predictions and practical applications. The findings demonstrated that increasing dielectric thickness significantly reduces gate leakage currents, with devices featuring a 30 nm Al_2O_3 layer achieving leakage current densities as low as 2.8×10^{-8} A/cm^2, while maintaining thermal stability up to 150 °C. However, this comes at the cost of reduced gate capacitance, which could potentially impact high-frequency performance. The lumped element modelling approach employed in this study accurately predicted these performance trends and provided a robust framework for optimizing gate stack design, with statistical validation ensuring the reliability of the results.

Building on these findings, several practical recommendations can be proposed to enhance the design and performance of GaN-based MIS-HEMTs. First, a dielectric thickness of 20–25 nm is recommended as an optimal balance between minimizing leakage currents and maintaining sufficient gate capacitance for high-frequency operations. This range ensures reliable operation under thermal stress, reducing the likelihood of performance degradation in high-power and high-temperature applications. Second, adopting advanced high-k materials, such as HfO_2 or ZrO_2, as alternatives to Al_2O_3, could further improve barrier resistance and thermal stability, as suggested by previous studies. These materials exhibit superior dielectric properties and can potentially reduce gate leakage currents while maintaining or enhancing capacitance. Third, implementing precision control over deposition techniques, such as atomic layer deposition (ALD), is essential for achieving uniform dielectric layers with minimal defects, ensuring consistent performance across devices.

Additionally, the study underscores the importance of interface engineering to enhance device stability and reliability. Techniques such as surface passivation and interface charge control can mitigate trapping effects, which often lead to threshold voltage instabilities and increased leakage currents. Manufacturers are encouraged to integrate these techniques during device fabrication to optimize gate stack quality and performance. The integration of advanced computational Modelling tools, such as the lumped element model demonstrated in this study, should also be standard practice in the design and analysis of GaN-based devices. These models provide valuable insights into the interactions between device parameters and operational conditions, enabling predictive design strategies that reduce development time and costs.

For industrial applications, adopting these recommendations could result in more reliable and efficient GaN-based MIS-HEMTs, suitable for deployment in high-power electronics, RF systems, and automotive applications. The findings also provide a foundation for future research into gate stack materials and configurations, encouraging further exploration of multi-layer dielectric stacks and novel barrier materials to enhance performance. Finally, these results advocate for closer collaboration between academia and industry to develop standardized testing protocols and modelling frameworks that address the challenges of optimizing GaN-based device performance.

This study not only advances the understanding of gate stack barrier resistance in GaN-based MIS-HEMTs but also provides actionable insights for optimizing device design. By combining rigorous experimental analysis with predictive modelling, the research lays the groundwork for the next generation of high-performance electronic devices, ensuring their adaptability and reliability in a rapidly evolving technological landscape. These practical recommendations, if implemented, hold the potential to significantly improve the efficiency, reliability, and scalability of GaN-based devices, paving the way for their widespread adoption in diverse high-performance applications.

References

1. Baliga BJ. Fundamentals of power semiconductor devices. Springer Science & Business Media; c2008.
2. Mishra UK, Parikh P, Yi-Feng W. AlGaN/GaN HEMTs—An overview of device operation and applications. Proc IEEE. 2002;90(6):1022-1031.
3. Higashiwaki M, Sasaki K, Kuramata A, Masui T, Yamakoshi S. Gallium oxide (Ga2O3) metal-semiconductor field-effect transistors on single-crystal β-Ga2O3 substrates. Appl Phys Lett. 2012;100(1):013504.
4. Khan MA, Balakrishnan K, Katona T. Ultraviolet light-emitting diodes based on group III nitrides. Nat Photonics. 2008;2(2):77-84.
5. Yang J, Li S, Shi Y, Lu W, Feng Z. High-temperature reliability of GaN-based MIS-HEMTs. Microelectron Reliab. 2010;50(9-11):1299-12303.
6. Kim Y, Kim H, Han D, *et al.* Interface engineering in GaN-based MIS-HEMTs: The role of dielectric material and processing. J Appl Phys. 2015;117(22):224504.
7. Li T, Chen X, Sun L, *et al*. Gate leakage current suppression in GaN MIS-HEMTs: A material and process perspective. IEEE Trans Electron Devices. 2017;64(1):143-150.
8. Zhou J, Wang S, Huang R, Chen Z. Dynamic behavior of gate leakage in GaN MIS-HEMTs under high-frequency operations. IEEE Electron Device Lett. 2018;39(6):846-849.
9. Chabak KD, Green BG, Miller N, *et al*. Enhancement-mode GaN HEMT reliability with Al2O3 passivation. IEEE Electron Device Lett. 2011;32(9):1245-1247.
10. Tanaka S, Okamoto T, Yamada K, *et al*. Gate dielectric material selection for GaN-based transistors. Appl Phys Express. 2012;5(9):094101.
11. Wang L, Zhang H, Wang Y, *et al*. Advanced gate stack designs for GaN MIS-HEMTs. Solid-State Electron. 2014;100:39-45.
12. Li S, Zhou Y, Zhang X, *et al*. Physics-based Modelling of GaN MIS-HEMTs. IEEE Trans Electron Devices. 2019;66(5):2236-2243.
13. Hori T. Gate Dielectrics and MOS ULSIs: Principles, Technologies and Applications. Springer; c1997.
14. Wang J, Luo J, Ding X, *et al*. Leakage current mechanisms in AlGaN/GaN MIS-HEMTs. Appl Phys Lett. 2014;105(6):062101.
15. Pan J, Chen T, Xu G, *et al*. Lumped-element equivalent circuit Modelling for GaN HEMTs. IEEE Trans Microw Theory Tech. 2016;64(1):33-43.
16. Tanaka T, Yamada S, Okamoto K, *et al*. Analysis of

trapping effects in GaN MIS-HEMTs. Appl Phys Lett. 2015;107(14):143501.
17. Wu T, Ren F, Wang H, *et al*. Gate stack engineering for reliability improvement in GaN MIS-HEMTs. Appl Phys Lett. 2017;111(7):072103.
18. Chu R, Li W, Zhou Z, *et al*. Thermal stability of gate stack in GaN MIS-HEMTs. IEEE Trans Device Mater Rel. 2018;18(1):56-63.
19. Chen X, Lu J, Liu P, *et al*. High-performance GaN-based MIS-HEMTs with optimized gate stack structure. Appl Phys Lett. 2016;108(15):152104.