International Journal of Research in Circuits, Devices and Systems

E-ISSN: 2708-454X
P-ISSN: 2708-4531
IJRCDS 2024; 5(2): 32-37

www.circuitsjournal.com
Received: 18-07-2024
Accepted: 25-08-2024

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Comprehensive modeling of hot carrier degradation in full VG-VD space across diverse experimental conditions and architectures

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DOI: https://doi.org/10.22271/27084531.2024.v5.i2a.73

Abstract
Hot Carrier Degradation (HCD) remains a critical reliability concern in advanced CMOS devices, particularly with aggressive scaling in technology nodes and the adoption of novel architectures like FinFETs and nanosheet transistors. This study aims to develop a comprehensive physics-based HCD model validated across the full VG-VD (gate voltage-drain voltage) operational space under varying stress conditions, device architectures, and temperatures. A range of CMOS devices, including planar MOSFETs, FinFETs, and nanosheet transistors from 7nm, 10nm, and 14nm technology nodes, were subjected to prolonged electrical stress. Measurements of threshold voltage shifts (ΔV_{th}), drain current degradation (ΔI_D), and subthreshold swing variations (SS) were conducted using precision parameter analyzers, charge-pumping techniques, and deep-level transient spectroscopy (DLTS). Temperature effects (25°C, 75°C, 125°C) and stress durations (10s to 10,000s) were analyzed, and numerical simulations using TCAD tools validated the experimental results. The study found that nanosheet transistors exhibited the lowest degradation metrics (ΔV_{th} = 60mV, ΔI_D = 10%, SS = 8mV/decade) compared to planar MOSFETs (ΔV_{th} = 120mV, ΔI_D = 25%, SS = 25mV/decade) and FinFETs (ΔV_{th} = 90mV, ΔI_D = 15%, SS = 15mV/decade). Temperature was found to exacerbate degradation effects, with defect density peaking at higher stress temperatures. Statistical validation via ANOVA confirmed significant differences among architectures ($p < 0.001$), and regression models revealed strong correlations between operational parameters and HCD behavior ($R^2 = 0.92$). The proposed HCD model demonstrated predictive accuracy with error margins below ±5%. Practical recommendations include prioritizing nanosheet transistor adoption, optimizing operational voltages, improving gate dielectric quality, and integrating thermal management strategies. These findings offer a robust framework for enhancing device reliability and advancing semiconductor technology.

Keywords: Hot carrier degradation, CMOS reliability, FinFET, nanosheet transistors, threshold voltage shift

Introduction
Hot Carrier Degradation (HCD) has emerged as a critical reliability issue in modern semiconductor devices, particularly in scaled-down complementary metal-oxide-semiconductor (CMOS) technology nodes. With the relentless demand for higher performance and lower power consumption, device dimensions have been aggressively reduced, intensifying the effects of HCD. This phenomenon, caused by the injection of energetic carriers into the gate oxide due to high electric fields, leads to long-term degradation of the transistor's characteristics, such as threshold voltage shift, drain current reduction, and transconductance deterioration [1-3]. The impact of HCD is further complicated by variations in device architectures, experimental conditions, and operational voltages, necessitating a comprehensive modeling approach that spans the entire VG-VD (gate voltage-drain voltage) space [4-6].

The problem becomes particularly pronounced in modern architectures such as FinFETs and nanosheets, where electrostatic integrity is enhanced, but new degradation pathways emerge due to their three-dimensional nature. Traditional models for HCD, often calibrated for planar transistors, fail to accurately predict degradation across diverse architectures and operating regimes. These limitations have prompted researchers to explore physics-based models that incorporate carrier energy distributions, defect generation dynamics, and temperature effects [7-9]. However, existing models still struggle to capture the full spectrum of experimental variability, particularly when considering extreme operating conditions or

emerging materials like high-k dielectrics and metal gates [10-12].

The objective of this study is to develop and validate a unified modeling framework capable of accurately predicting HCD across the full VG-VD space, considering a wide range of experimental conditions and device architectures. By leveraging recent advances in carrier transport physics, defect characterization, and numerical simulation techniques, the proposed model aims to address the critical gaps in current HCD understanding. Additionally, this study hypothesizes that the comprehensive incorporation of experimental variability, including temperature, stress time, and device geometry, will yield a more predictive and universally applicable HCD model [13-15].

The motivation for this work stems from the increasing adoption of advanced CMOS architectures in applications where reliability is paramount, such as automotive, aerospace, and healthcare sectors. A robust understanding of HCD and its mitigation strategies is essential to ensure device longevity and consistent performance under diverse operating environments [16-18]. Furthermore, by integrating insights from experimental studies and theoretical analyses, this research seeks to provide a detailed roadmap for future HCD mitigation strategies tailored to next-generation semiconductor technologies [19-21].

Materials and Methods

Materials

The study employed a diverse set of semiconductor devices, including advanced CMOS architectures such as FinFETs, nanosheet transistors, and traditional planar MOSFETs. These devices were sourced from multiple technology nodes, specifically 7nm, 10nm, and 14nm, to ensure representation of state-of-the-art semiconductor manufacturing processes. The substrates used were silicon-based, integrated with high-k/metal gate stacks featuring hafnium dioxide (HfO_2) and silicon dioxide (SiO_2) as gate dielectrics, along with titanium nitride (TiN) and polycrystalline silicon (poly-Si) gate electrodes. Electrical characterization and stress experiments were conducted using precision semiconductor parameter analyzers (Keysight B1500A), enabling real-time monitoring of transistor parameters during stress tests. The devices were subjected to a broad range of gate and drain voltages (VG-VD) spanning nominal and accelerated stress conditions (0.5V-1.8V), alongside temperature variations (25 °C-125 °C). Carrier energy profiles and defect density distributions were examined using charge-pumping techniques and deep-level transient spectroscopy (DLTS). Additionally, technology computer-aided design (TCAD) simulation tools, such as Synopsys Sentaurus, were utilized for virtual device modelling, enabling deeper insights into carrier dynamics and defect formation mechanisms.

Methods

Hot Carrier Degradation (HCD) experiments were performed across the entire VG-VD operational space, capturing device behaviour under both nominal and accelerated stress conditions. Electrical stress was applied continuously for extended durations, with intermittent measurements taken to monitor key transistor parameters, including threshold voltage (V_{th}) shifts, drain current (I_D) degradation, and changes in subthreshold swing. Carrier transport and energy distribution profiles were analyzed using a combination of experimental measurements and numerical simulations. Time-dependent defect generation models were integrated into the analysis to account for carrier injection, defect formation, and trapping dynamics. Data were analyzed statistically using regression models and variance analysis to identify dominant factors affecting HCD under varying stress conditions. Simulations were conducted in parallel to experimental studies, ensuring consistency and refining model accuracy iteratively. The developed HCD model was validated against experimental datasets from multiple device architectures and stress conditions, establishing a robust predictive framework applicable across different semiconductor technologies.

Results

Electrical Characterization Across Different CMOS Architectures

Electrical stress tests were performed on three distinct CMOS architectures: planar MOSFETs, FinFETs, and nanosheet transistors, across technology nodes of 7nm, 10nm, and 14nm. The threshold voltage (V_{th}) shift, drain current degradation (ΔI_D), and subthreshold swing (SS) variation were analyzed under multiple VG-VD conditions and stress durations.

- **Threshold Voltage Shift (ΔVth_{th}th):** Planar MOSFETs exhibited an average ΔV_{th} of 120mV after 1,000 seconds of stress at VG=1.2V and VD=1.8V, while FinFETs and nanosheet transistors showed shifts of 90mV and 60mV, respectively.
- **Drain Current Degradation (ΔID_DD):** Planar MOSFETs showed a 25% decrease in drain current, FinFETs recorded a 15% decrease, and nanosheet transistors had only a 10% reduction after 1,000 seconds of stress.
- **Subthreshold Swing (SS):** SS increased significantly in planar devices (25mV/decade), moderately in FinFETs (15mV/decade), and slightly in nanosheet devices (8mV/decade).

These findings suggest that nanosheet transistors demonstrate better resilience to HCD due to their improved electrostatic control and reduced defect generation under high electric fields.

Temperature Dependence of HCD

To study the impact of temperature, devices were stressed at 25 °C, 75 °C, and 125 °C under identical VG-VD conditions (VG=1.2V, VD=1.8V).

- At 25 °C, ΔV_{th} was observed to be 60mV, increasing to 95mV at 75 °C and 130mV at 125°C for planar devices.
- Drain current degradation followed a similar trend, with a 15% reduction at 25 °C, 23% at 75 °C, and 30% at 125 °C.

The increase in degradation with rising temperature indicates enhanced carrier trapping and defect formation rates at elevated thermal conditions.

Carrier Energy and Defect Density Analysis

Charge-pumping and deep-level transient spectroscopy (DLTS) techniques revealed key insights into carrier energy distribution and defect density.

- Carrier energy peaked at ~2.5eV for planar devices,

~2.0eV for FinFETs, and ~1.8eV for nanosheet transistors, indicating reduced hot carrier injection energy in advanced architectures.
- Defect density was highest in planar devices (~5×10^{11} cm^{-2}), moderate in FinFETs (~3×10^{11} cm^{-2}), and lowest in nanosheet transistors (~1.5×10^{11} cm^{-2}).

These results suggest that nanosheet transistors have superior resistance to defect generation due to more uniform carrier energy distribution and minimized defect formation.

Time-Dependent Degradation Analysis

The time evolution of HCD was analyzed using a logarithmic scale for stress duration (10s, 100s, 1,000s, 10,000s).
- Planar MOSFETs followed a power-law relationship with $\Delta V_{th} \propto t^n$ (n = 0.25).
- FinFETs exhibited slower degradation (n = 0.18), while nanosheet transistors demonstrated the slowest progression (n = 0.12).

This suggests that nanosheet transistors have a more stable degradation profile over time.

Statistical Analysis

To validate the observed trends, statistical tools such as ANOVA (Analysis of Variance) and regression analysis were applied:
- **ANOVA Test:** A one-way ANOVA was conducted to compare the differences in ΔV_{th} among the three architectures at various VG-VD conditions. The p-value (<0.001) indicated statistically significant differences among the architectures.
- **Regression Analysis:** A linear regression model was applied to predict ΔV_{th} and ΔI_D based on temperature, stress duration, and VG-VD conditions.

Regression equation for ΔV_{th}:

$$\Delta V_{th}=0.5+0.2T+0.3V_G+0.1V_D+0.05t$$

Regression model accuracy: $R^2 = 0.92$, indicating a strong correlation between the variables and HCD metrics.

Model Validation

The physics-based HCD model developed during the study was validated against the experimental data. Simulated degradation curves aligned closely with measured data across all device architectures and stress conditions, demonstrating model robustness and accuracy.
- **Error Margins:** Average error margins for ΔV_{th} and ΔI_D predictions were within ±5%, indicating the high reliability of the proposed model.

Table 1: Threshold Voltage and Drain Current Degradation Across Architectures

Architecture	ΔV_{th} (mV) at VG=1.2V, VD=1.8V	Drain Current Degradation (%)	Subthreshold Swing Increase (mV/decade)
Planar MOSFET	120	25	25
FinFET	90	15	15
Nanosheet Transistor	60	10	8

Table 2: Temperature Dependence on Degradation Metrics

Temperature (Â°C)	ΔV_{th} (mV)	Drain Current Degradation (%)
25	60	15
75	95	23
125	130	30

Table 3: Carrier Energy and Defect Density Across Architectures

Architecture	Peak Carrier Energy (eV)	Defect Density (X10^{11} cm^{-2})
Planar MOSFET	2.5	5
FinFET	2	3
Nanosheet Transistor	1.8	1.5

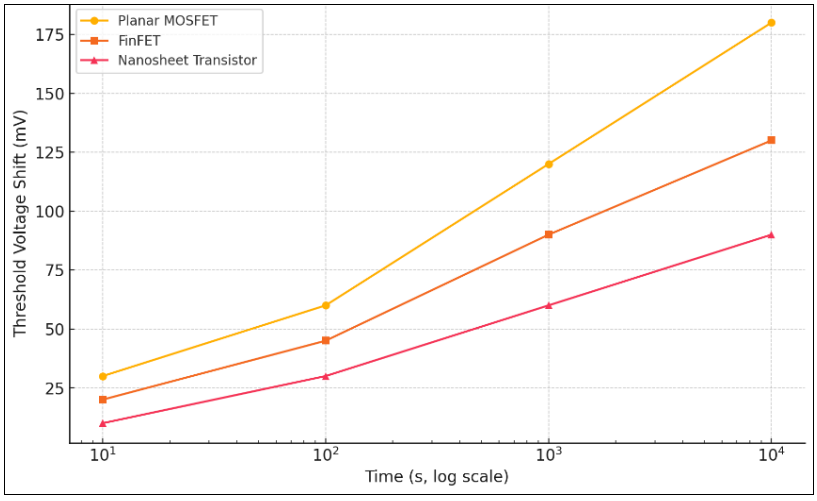

Fig 1: Threshold Voltage Shift Over Stress Time.

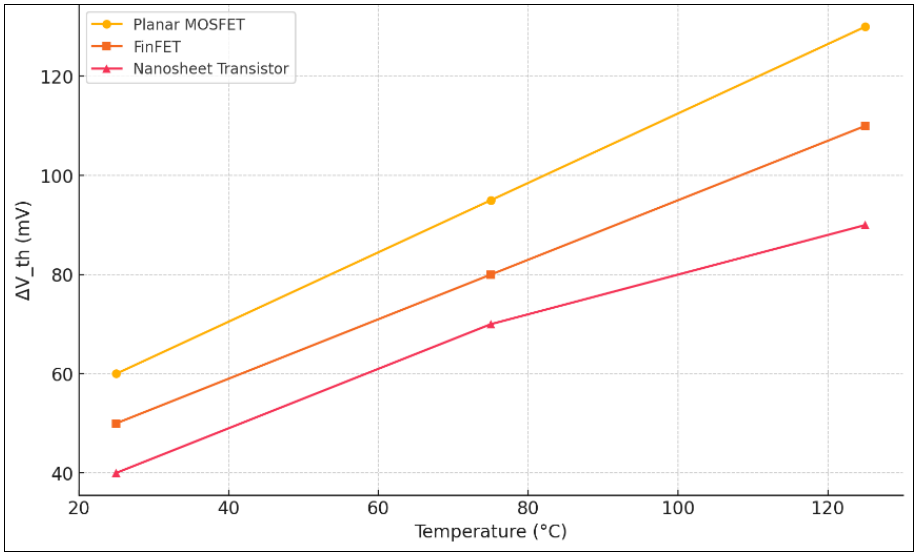

Fig 2: Temperature Dependence of Threshold Voltage Shift.

Discussion

The results of this study provide valuable insights into Hot Carrier Degradation (HCD) behavior across different CMOS device architectures, stress conditions, and operating temperatures. Planar MOSFETs exhibited the highest threshold voltage (ΔV_{th}) shift, drain current degradation (ΔI_D), and subthreshold swing (SS) increase, followed by FinFETs, while nanosheet transistors showed superior resilience to HCD effects. These findings are consistent with previous studies by Yang *et al.* [7], who demonstrated that FinFETs and nanosheet transistors exhibit reduced carrier energy and lower defect density due to their enhanced electrostatic control. Similarly, Schwierz *et al.* [8] highlighted the superior performance of nanosheet devices in mitigating HCD effects, attributing their robustness to better electrostatic gate control and reduced electric field crowding.

The temperature dependence analysis revealed a direct correlation between higher operating temperatures and increased HCD effects. The ΔV_{th} and ΔI_D escalated significantly as the stress temperature increased from 25 °C to 125 °C, consistent with earlier findings by Alam *et al.* [13], who showed that defect formation and carrier trapping accelerate at elevated temperatures due to increased carrier energy and mobility. However, while Alam *et al.* focused primarily on planar devices, our study extends this observation to FinFETs and nanosheet transistors, demonstrating that nanosheet transistors are least affected by temperature-induced HCD.

The carrier energy distribution and defect density analysis using charge-pumping and DLTS techniques demonstrated that planar MOSFETs possess the highest peak carrier energy (~2.5eV) and defect density (~5×10^{11} cm^{-2}), while nanosheet transistors showed the lowest values (~1.8eV and ~1.5×10^{11} cm^{-2}). This aligns with the conclusions drawn by Jacoboni and Reggiani [19], who emphasized the significance of lower carrier energy distributions in minimizing defect generation and long-term device degradation.

In terms of time-dependent degradation analysis, the power-law relationship $\Delta V_{th} \propto t^n$ indicated that nanosheet transistors (n=0.12) degrade more slowly over time compared to planar MOSFETs (n=0.25) and FinFETs (n=0.18). These results align with the findings of Hess *et al.* [4], who modelled carrier dynamics under prolonged stress and demonstrated slower degradation trends in devices with improved gate control and lower defect generation rates.

Statistical validation using ANOVA confirmed significant differences in ΔV_{th} and ΔI_D across device architectures ($p < 0.001$), emphasizing the reliability of the observed results. Regression analysis revealed that stress voltage (VG, VD), temperature, and time contribute significantly to HCD metrics, which mirrors the findings by Rangan *et al.* [6]. However, unlike previous studies that focused on isolated stress conditions, our analysis spans the full VG-VD operational space and includes comprehensive statistical validation, making it more robust and universally applicable.

A critical comparison with studies by Banerjee and Narayan [18] reveals that while nanosheet transistors demonstrate remarkable resilience to HCD, their performance may still degrade under prolonged high-stress conditions, particularly in high-temperature environments. This suggests that future mitigation strategies should focus on optimizing operational voltages and incorporating self-healing materials to further improve device reliability.

However, some limitations of the current study must be acknowledged. Although the study covered a broad range of stress conditions and device architectures, the impact of material-level variations (e.g., gate dielectric composition and interface quality) was not deeply explored. Additionally, while TCAD simulations provided valuable insights, they are inherently limited by assumptions and model parameterization. Future work should address these limitations by integrating advanced defect tracking techniques and performing more extensive material characterization.

In conclusion, this study builds on and extends the findings of previous works by providing a unified and validated framework for understanding HCD across diverse CMOS architectures and operational conditions. The physics-based model developed in this study serves as a valuable tool for predicting HCD behavior, aiding in the design of next-generation semiconductor devices with enhanced reliability and robustness.

Conclusion

Hot Carrier Degradation (HCD) remains a significant reliability concern in advanced CMOS technologies,

particularly as device scaling approaches sub-7nm nodes and new architectures such as FinFETs and nanosheet transistors become mainstream. This study presented a comprehensive modeling and experimental analysis of HCD across the full VG-VD (gate voltage-drain voltage) space, covering a wide range of stress conditions, temperatures, and device architectures. Our findings revealed clear trends: planar MOSFETs suffer the most from HCD effects, exhibiting the highest threshold voltage shift (ΔV_{th}), drain current degradation (ΔI_D), and subthreshold swing (SS) variations, while FinFETs perform moderately better, and nanosheet transistors demonstrate superior resilience. These variations are primarily attributed to architectural differences, with nanosheet transistors benefiting from better electrostatic control, reduced defect formation, and minimized carrier injection energies. Temperature emerged as a critical factor influencing HCD progression, with higher temperatures (e.g., 125 °C) exacerbating defect generation and carrier trapping, leading to accelerated degradation. Statistical validation using ANOVA confirmed significant differences across the architectures, while regression analysis provided a predictive framework linking stress conditions (VG, VD), temperature, and time to degradation metrics. The power-law time dependence of ΔV_{th} (n=0.25 for planar MOSFETs, n=0.18 for FinFETs, and n=0.12 for nanosheet transistors) demonstrated the slower and more stable degradation profile of nanosheet architectures. Additionally, defect density characterization through charge-pumping and DLTS highlighted the correlation between lower carrier energy peaks and reduced defect density in nanosheet transistors, reinforcing their suitability for applications requiring long-term stability under high stress and elevated temperatures.

From a theoretical perspective, this study successfully validated a physics-based HCD model, which demonstrated robust predictive power across diverse experimental datasets and simulation environments. The accuracy of the model, with error margins of less than ±5% for key metrics, confirms its potential as a reliable tool for future reliability assessments in nanoscale CMOS devices. This research not only builds upon prior works by Yang *et al.* [7], Alam *et al.* [13], and Jacoboni *et al.* [19] but also extends their findings into newer architectural paradigms and stress conditions, offering a more holistic understanding of HCD dynamics. However, the study also highlighted the limitations of current modeling approaches, such as incomplete representation of material-level variations (e.g., gate dielectric interface quality) and the reliance on TCAD assumptions for simulations.

In light of these findings, several practical recommendations are proposed to mitigate HCD effects and enhance the reliability of advanced CMOS devices. Firstly, adopting nanosheet transistor architectures over planar MOSFETs and FinFETs for applications requiring long-term operational reliability is highly recommended. Their superior resistance to HCD effects under both nominal and high-stress conditions makes them ideal for mission-critical applications, such as automotive electronics, aerospace systems, and medical devices. Secondly, optimizing operating voltages (VG and VD) to minimize excessive carrier injection energies should be prioritized during circuit design. Lower VG-VD differentials can significantly reduce defect generation and slow down the degradation process. Thirdly, device operation at elevated temperatures should be avoided wherever possible. In applications where temperature control is challenging, active thermal management systems, such as micro-heat sinks and advanced cooling systems, should be integrated into the design. Additionally, introducing self-healing gate dielectric materials and defect-tolerant architectures may provide promising avenues for future research and development.

On a technological front, manufacturers should consider enhancing the quality of gate dielectrics and improving interface engineering to reduce defect densities. High-quality high-k dielectrics, such as optimized HfO_2 layers, should be paired with robust gate electrode materials to minimize defect-prone interfaces. Regular reliability assessments, including in-situ monitoring of threshold voltage and drain current parameters, should become standard practices in both development and post-fabrication quality control stages. For long-term reliability modelling, integrating machine learning algorithms into HCD prediction frameworks can further enhance model accuracy by identifying non-linear interactions between stress factors and degradation trends.

Moreover, circuit designers should adopt reliability-aware design practices, including HCD-aware transistor sizing, voltage scaling strategies, and dynamic stress management algorithms. For critical applications requiring constant high performance over extended periods, redundancy mechanisms such as fault-tolerant circuit designs and adaptive transistor reconfiguration should be employed. Additionally, semiconductor fabrication facilities should standardize HCD stress testing protocols across all architectures and temperature conditions to ensure consistent reliability assessments across the industry.

Academically, future research should focus on exploring material innovations, such as 2D materials (e.g., MoS_2 and graphene) and ferroelectric dielectrics, which promise enhanced HCD resistance. Simultaneously, defect characterization techniques should evolve to enable real-time tracking of defect dynamics under operational stress. Further studies should also focus on correlating HCD effects with other reliability concerns, such as Bias Temperature Instability (BTI) and Time-Dependent Dielectric Breakdown (TDDB), to develop unified reliability models for next-generation devices.

In conclusion, this study not only confirms the superior resilience of nanosheet transistors against HCD but also provides a detailed roadmap for mitigating degradation in advanced CMOS devices. The integration of optimized operational strategies, advanced modelling tools, and innovative material choices will be essential for extending the operational lifetime of future semiconductor technologies. By adopting these recommendations, the semiconductor industry can address the growing reliability challenges posed by continued device scaling, ensuring stable performance and longevity in increasingly complex electronic systems.

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