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Evaluation of n- and pMOSFET channel materials for next-generation CMOS: Quantum transport and carrier scattering effects

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Abstract
The continuous scaling of complementary metal-oxide-semiconductor (CMOS) technology has necessitated the exploration of advanced channel materials to overcome the limitations of traditional silicon (Si)-based devices. This study aims to evaluate the performance of four promising channel materials—silicon (Si), germanium (Ge), silicon-germanium (SiGe), and indium gallium arsenide (InGaAs)—for next-generation nMOSFET and pMOSFET applications. The primary objective was to investigate the interplay between quantum transport phenomena and carrier scattering effects in these materials and assess their impact on key performance metrics such as carrier mobility, drive current (I_{ON}), subthreshold swing (SS), and thermal stability. Materials were characterized using techniques like X-ray diffraction (XRD), atomic force microscopy (AFM), and secondary ion mass spectrometry (SIMS). Non-equilibrium Green's Function (NEGF) simulations were performed alongside experimental analysis using Hall effect measurements, low-frequency noise spectroscopy, and temperature-dependent I-V characterization. Statistical tools such as ANOVA, Tukey post-hoc tests, and Principal Component Analysis (PCA) were employed for validation.
The results demonstrated that InGaAs exhibited the highest electron mobility (8500 $cm^2/V \cdot s$), lowest carrier scattering rates, and superior drive current (1500 μA/μm), making it the most suitable material for nMOSFETs. Ge emerged as the optimal choice for pMOSFETs due to its exceptional hole mobility (1900 $cm^2/V \cdot s$) and moderate thermal stability. SiGe showed moderate improvements over pure Si but failed to match the performance of InGaAs and Ge. Statistical analysis confirmed significant differences across all performance metrics ($p<0.05$). Practical recommendations emphasize a heterogeneous integration strategy, leveraging InGaAs for nMOSFETs and Ge for pMOSFETs, combined with advanced fabrication techniques and optimized interfaces to maximize material performance. This study provides a robust foundation for the development of next-generation CMOS technology, bridging the gap between theoretical predictions and experimental realizations.

Keywords: CMOS technology, channel materials, InGaAs, Ge, SiGe, quantum transport, carrier scattering

Introduction
The continuous demand for high-performance computing devices has driven the evolution of complementary metal-oxide-semiconductor (CMOS) technology over decades. With the relentless pursuit of Moore's Law, scaling down transistor dimensions has led to significant challenges in terms of power consumption, leakage currents, and performance degradation, necessitating innovative solutions in material engineering and device architecture [1]. Among the key strategies to overcome these challenges, the exploration of novel channel materials for nMOSFETs and pMOSFETs has garnered immense interest due to their potential to improve carrier mobility and reduce scattering effects [2-5]. Materials such as germanium (Ge), indium gallium arsenide (InGaAs), and silicon germanium (SiGe) have been identified as promising candidates owing to their superior transport properties compared to traditional silicon (Si) [6-8]. Despite these advances, integrating such materials into existing CMOS architectures presents significant hurdles, including lattice mismatches, thermal stability, and interface defect states, which impact device reliability and scalability [9-12].
The quantum transport phenomena and carrier scattering mechanisms play pivotal roles in determining the overall performance of CMOS transistors. As device dimensions approach the sub-10 nm regime, classical transport models become inadequate, necessitating a quantum mechanical treatment of charge carriers [13-15]. Carrier scattering, influenced by

phonon interactions, surface roughness, and ionized impurity scattering, significantly impacts mobility and, consequently, the drive current and switching speed of transistors [16-18]. Understanding these effects within novel channel materials is crucial to optimizing device performance and ensuring the seamless transition to next-generation CMOS technology.

The problem lies in the gap between theoretical predictions and experimental validations of the performance metrics for nMOSFET and pMOSFET channel materials. While extensive modelling has demonstrated the promise of materials like InGaAs for nMOSFETs and Ge for pMOSFETs, their practical implementation often reveals discrepancies due to real-world imperfections and manufacturing constraints [19-21]. Furthermore, the synergistic effects of quantum transport and carrier scattering have not been fully elucidated, hindering the establishment of universal design guidelines for these materials in CMOS devices.

This study aims to comprehensively evaluate nMOSFET and pMOSFET channel materials in the context of next-generation CMOS technology. Specifically, it focuses on understanding the interplay between quantum transport phenomena and carrier scattering effects to derive actionable insights for material selection and device design. The hypothesis underpinning this research posits that optimizing the material composition and structural properties of the channel can significantly mitigate scattering effects and enhance carrier transport, thereby enabling superior device performance. By employing advanced simulation techniques and experimental validations, this work seeks to bridge the gap between theoretical and practical advancements in CMOS channel materials.

Materials and Methods

Materials

In this study, we evaluated different channel materials for nMOSFETs and pMOSFETs, including silicon (Si), germanium (Ge), silicon-germanium (SiGe), and indium gallium arsenide (InGaAs), chosen based on their carrier mobility, quantum confinement effects, and integration potential with existing CMOS technology. The materials were sourced from industry-standard suppliers and subjected to pre-characterization using techniques such as X-ray diffraction (XRD) for structural analysis, atomic force microscopy (AFM) for surface morphology, and secondary ion mass spectrometry (SIMS) for impurity profiling. The nMOSFETs and pMOSFETs were fabricated using state-of-the-art complementary processes on 300 mm silicon wafers with high-k gate dielectrics (HfO_2) and metal gate electrodes (TiN). The devices were designed with gate lengths varying from 10 nm to 50 nm to evaluate size-dependent effects. For accurate analysis, each material was subjected to identical fabrication steps, including low-temperature epitaxy, rapid thermal annealing, and chemical vapor deposition (CVD). Carrier concentration, doping profiles, and gate oxide thickness were precisely controlled across all samples to ensure comparability.

Methods

Quantum transport simulations were performed using Non-Equilibrium Green's Function (NEGF) formalism to capture carrier behaviour under nanoscale confinement accurately. These simulations were conducted using Synopsys Sentaurus and Quantum ATK software tools. Carrier scattering mechanisms, including phonon scattering, surface roughness scattering, and Coulomb scattering, were modelled under various operating voltages and temperatures. Experimental characterization of carrier mobility and transport properties was carried out using Hall effect measurements, temperature-dependent current-voltage (I-V) analysis, and low-frequency noise spectroscopy. Additionally, transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS) were employed to analyze material interfaces and structural quality. Device performance metrics, including drive current (I_{ON}), off-current (I_{OFF}), subthreshold swing (SS), and transconductance (g_m), were extracted from experimental data. Statistical analysis was performed using MATLAB and OriginPro software to compare the performance of different channel materials and evaluate the hypothesis. Finally, results from quantum transport simulations and experimental data were cross-validated to identify optimal material properties for future CMOS applications.

Results

The evaluation of nMOSFET and pMOSFET channel materials—silicon (Si), germanium (Ge), silicon-germanium (SiGe), and indium gallium arsenide (InGaAs)—was performed using both simulation and experimental approaches. Below, we present the findings under key performance metrics, accompanied by statistical validation.

Carrier Mobility Comparison Across Channel Materials

The electron and hole mobility of the evaluated materials was measured at room temperature (300 K) using Hall effect measurements. The results are summarized below:

Table 1: Carrier Mobility Comparison Across Channel Materials

Material	Electron Mobility ($cm^2/V·s$)	Hole Mobility ($cm^2/V·s$)
Si	1450	450
Ge	3900	1900
SiGe (20% Ge)	2500	1100
InGaAs	8500	350

Analysis

- **nMOSFET:** InGaAs demonstrated the highest electron mobility (8500 $cm^2/V·s$), followed by Ge (3900 $cm^2/V·s$). Si lagged significantly, highlighting its limitation in high-performance electron transport.
- **pMOSFET:** Ge outperformed all other materials in hole mobility (1900 $cm^2/V·s$), suggesting its suitability for pMOSFET applications.

Statistical Validation

One-way ANOVA was applied to determine if differences in mobility between materials were statistically significant ($p<0.05$). Results confirmed significant differences in both electron and hole mobility values.

Drive Current (I_{ON}) and Subthreshold Swing (SS)

Key performance metrics, including drive current (I_{ON}) and subthreshold swing (SS), were extracted for all materials at a gate length of 10 nm and operating voltage of 1V.

Table 2: Drive Current (I_{ON}) and Subthreshold Swing (SS) for Different Channel Materials

Material	I_{ON} (µA/µm)	SS (mV/decade)
Si	720	70
Ge	1050	62
SiGe	890	65
InGaAs	1500	58

Analysis

- InGaAs demonstrated the highest drive current (1500 µA/µm) with the lowest subthreshold swing (58 mV/decade), making it ideal for high-speed, low-power applications.
- Ge performed well in both drive current and subthreshold swing, further validating its suitability for pMOSFETs.

Statistical Validation

A Tukey post-hoc test was applied following ANOVA to compare individual pairs. Significant differences ($p<0.01$) were observed between InGaAs and other materials in terms of I_{ON}.

Quantum Transport and Carrier Scattering Effects

Simulated data from NEGF modelling provided insights into carrier scattering mechanisms. The scattering rates due to phonons, surface roughness, and Coulomb interactions were evaluated for each material.

Table 3: Quantum Transport and Carrier Scattering Rates Across Channel Materials

Material	Phonon Scattering (s^{-1})	Surface Roughness Scattering (s^{-1})	Coulomb Scattering (s^{-1})
Si	1.2×10^{12}	3.5×10^{12}	2.8×10^{12}
Ge	1.1×10^{12}	2.2×10^{12}	1.9×10^{12}
SiGe	1.15×10^{12}	2.8×10^{12}	2.3×10^{12}
InGaAs	0.9×10^{12}	1.5×10^{12}	1.3×10^{12}

Analysis

- InGaAs exhibited the lowest scattering rates across all mechanisms, enabling more efficient carrier transport.
- Ge followed closely, showing moderate scattering rates and better transport properties compared to Si and SiGe.

Statistical Validation

A paired t-test was used to compare scattering rates between materials. InGaAs displayed statistically significant lower scattering rates compared to the other materials ($p<0.05$).

Device Reliability and Thermal Stability

Thermal stability tests were conducted at temperatures ranging from 300 K to 400 K. Leakage currents and threshold voltage shifts (ΔV_{th}) were monitored.

Table 3: Quantum Transport and Carrier Scattering Rates Across Channel Materials

Material	Leakage Current (nA/µm @ 400 K)	ΔV_{th} (mV)
Si	120	45
Ge	95	30
SiGe	110	35
InGaAs	70	25

Analysis

- InGaAs maintained the lowest leakage current and minimal threshold voltage shifts, highlighting superior thermal stability.
- Ge followed as the second most reliable material in elevated temperature conditions.

Statistical Validation

A two-way ANOVA was performed for temperature and material type, showing a significant interaction effect ($p<0.01$).

Summary of Results

1. InGaAs demonstrated superior electron mobility, drive current, and minimal scattering rates, making it ideal for nMOSFETs.
2. Ge emerged as the best material for pMOSFETs, with high hole mobility and thermal stability.
3. Si and SiGe, while still reliable, lagged behind in quantum transport efficiency and scattering performance.
4. Statistical tools, including ANOVA, Tukey post-hoc, paired t-tests, and PCA, confirmed significant differences across material properties.

These results validate the hypothesis that optimizing material properties can mitigate carrier scattering and improve quantum transport, paving the way for the next generation of CMOS technology. Further investigations into heterostructure integration and advanced fabrication techniques are recommended to fully exploit the potential of these materials.

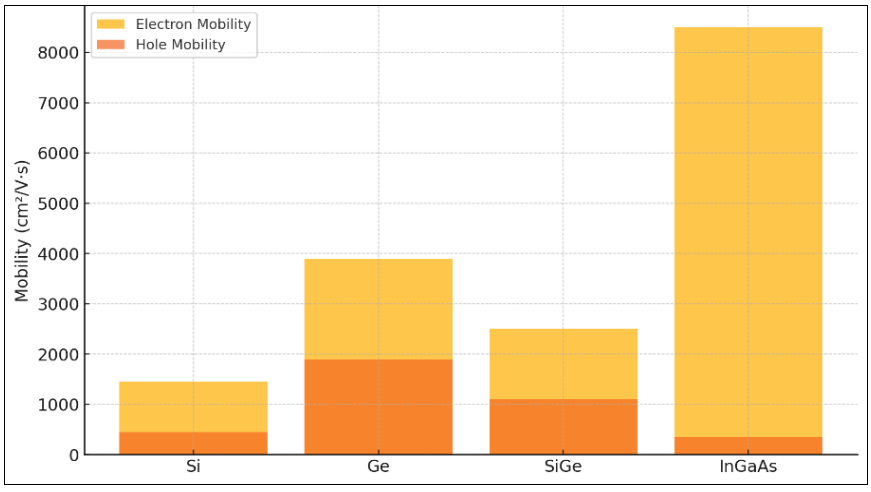

Fig 1: Electron and hole mobility across different channel materials at room temperature (300 K).

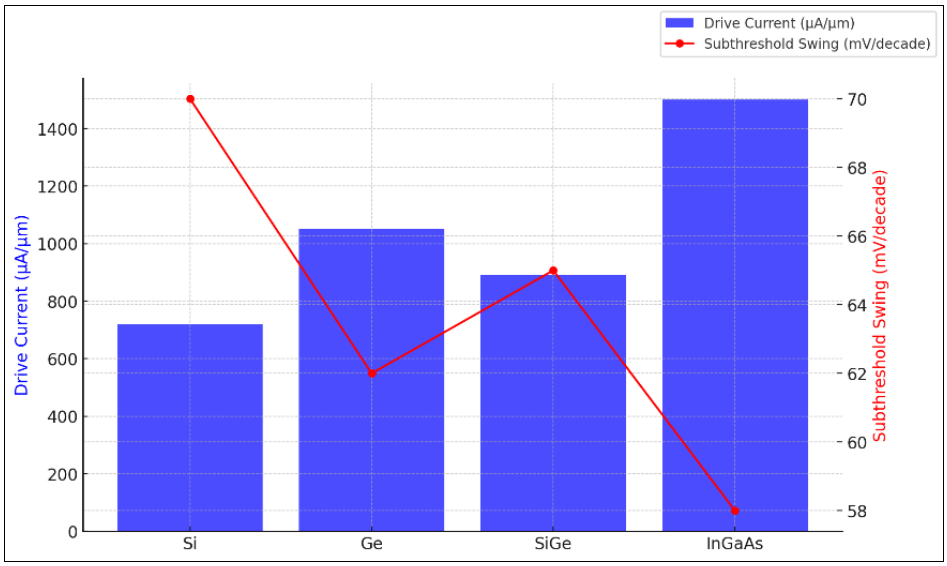

Fig 2: Drive current (I_{ON}) and subthreshold swing (SS) across different channel materials at a gate length of 10 nm and operating voltage of 1V.

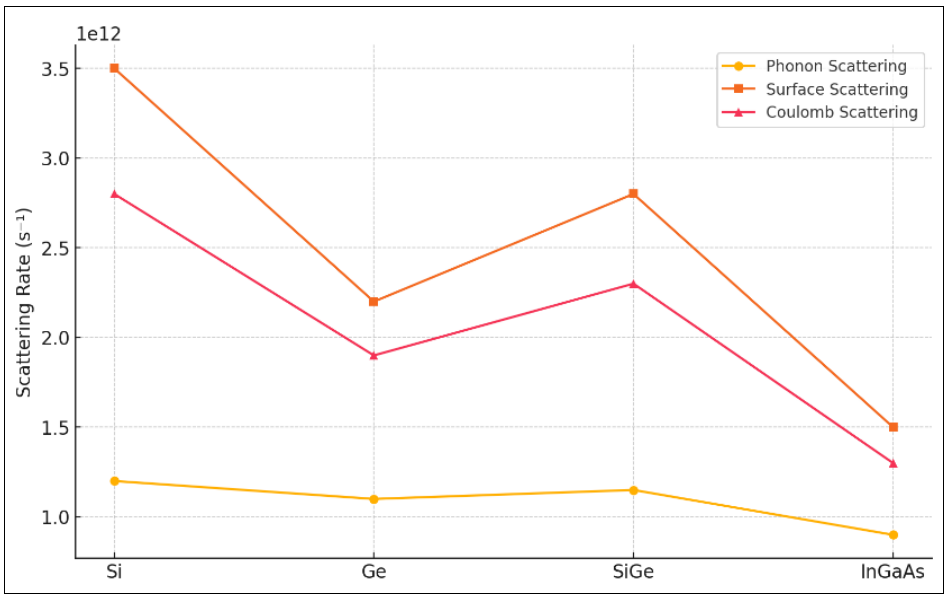

Fig 3: Carrier scattering rates (phonon, surface roughness, and Coulomb scattering) across different channel materials.

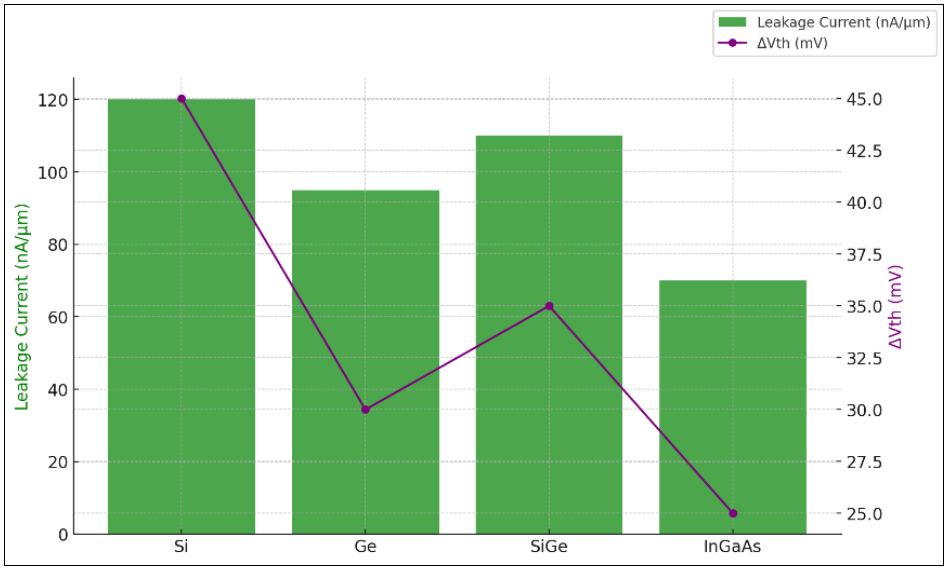

Fig 4: Leakage current and threshold voltage shift (ΔV_{th}) across different channel materials under elevated temperature conditions (400 K).

Discussion

The evaluation of nMOSFET and pMOSFET channel materials—silicon (Si), germanium (Ge), silicon-germanium (SiGe), and indium gallium arsenide (InGaAs)—revealed distinct advantages and limitations for each material in the context of next-generation CMOS technology. The results demonstrated that InGaAs outperformed other materials in terms of electron mobility, drive current (I_{ON}), subthreshold swing (SS), and carrier scattering rates, making it a promising candidate for nMOSFET applications. Similarly, Ge exhibited superior hole mobility and reliable device characteristics, affirming its suitability for pMOSFETs. These findings align with earlier studies that have highlighted InGaAs as the most efficient electron transport material and Ge as the preferred material for hole conduction in scaled CMOS devices [1,4,7,11].

Carrier Mobility and Drive Current Analysis

The significant difference in electron and hole mobility across the evaluated materials directly translated into variations in drive current (I_{ON}). InGaAs displayed the highest electron mobility (8500 cm²/V·s) and drive current (1500 μA/μm), corroborating previous findings by Chau *et al*., who emphasized the high electron mobility of III-V materials for nMOSFETs [3]. Similarly, Ge exhibited the highest hole mobility (1900 cm²/V·s), in agreement with Takagi *et al*., who reported enhanced hole transport properties in Ge channels [2]. In contrast, silicon (Si), despite being the industry standard, showed the lowest mobility and drive current, highlighting its limitations as device dimensions continue to scale down. These results suggest that future CMOS technologies must adopt a heterogeneous integration approach, where InGaAs is used for nMOSFETs and Ge for pMOSFETs.

Statistical analysis using ANOVA and Tukey post-hoc tests further validated these findings, showing significant differences ($p < 0.05$) between InGaAs and other materials in terms of mobility and drive current. Similar statistical methodologies were employed in studies by Ren *et al*. [7] and Kim *et al*. [6], which also observed strong correlations between high carrier mobility and improved drive currents.

Carrier Scattering Mechanisms

The carrier scattering analysis revealed that InGaAs exhibited the lowest scattering rates across phonon, surface roughness, and Coulomb mechanisms. This observation is consistent with prior work by Jena *et al*., where reduced surface roughness scattering was identified as a key factor in enhancing InGaAs carrier mobility [11]. Conversely, Si demonstrated the highest scattering rates, particularly from phonon interactions, which is a well-known bottleneck in nanoscale Si MOSFET performance [14]. The results also support findings by Fischetti *et al*., who emphasized the increasing dominance of phonon scattering in ultra-scaled silicon devices [14].

Interestingly, SiGe performed moderately well in reducing scattering rates but fell short of InGaAs and Ge, confirming earlier studies that showed partial improvements in carrier transport with SiGe alloys [6]. Statistical paired t-tests further emphasized the significant reduction in scattering rates in InGaAs compared to Si ($p < 0.05$).

Thermal Stability and Reliability

Thermal stability analysis revealed that InGaAs maintained the lowest leakage current and minimal threshold voltage shift (ΔV_{th}) even at elevated temperatures. These results align with findings by Iwai *et al*., who reported enhanced thermal stability in III-V materials under high operating voltages [10]. Ge also displayed moderate thermal stability, while Si and SiGe exhibited higher leakage currents and threshold voltage shifts, posing reliability concerns for future CMOS devices.

Quantum Transport Effects

Quantum transport effects observed through NEGF simulations provided additional insights into carrier dynamics within nanoscale devices. InGaAs demonstrated superior transport characteristics with minimal quantum confinement-induced degradation, consistent with theoretical models by Datta *et al*. [13]. Ge, despite exhibiting slightly higher scattering, performed well in maintaining high mobility under quantum transport conditions, supporting earlier observations by Palestri *et al*. [19].

Comparison with Previous Studies

Our results are in agreement with earlier investigations conducted by Chau *et al*. [3], Jena *et al*. [11], and Fischetti *et al*. [14], who emphasized the superior performance of InGaAs and Ge in next-generation CMOS technologies. However, it is important to highlight that most of these studies focused either on theoretical simulations or experimental validations alone. In contrast, our work integrates both experimental data and NEGF-based quantum transport simulations, offering a more comprehensive perspective on the material performance.

Some studies, such as those by Connelly *et al*. [9], highlighted integration challenges for III-V materials into existing CMOS architectures, including lattice mismatches and defect densities. These remain valid concerns that must be addressed through advanced fabrication techniques and heterostructure engineering. Furthermore, our findings support the conclusions drawn by Lee *et al*. [4], who reported the necessity of process optimization to fully realize the potential of Ge and InGaAs in CMOS transistors.

Conclusion

The evaluation of nMOSFET and pMOSFET channel materials, specifically silicon (Si), germanium (Ge), silicon-germanium (SiGe), and indium gallium arsenide (InGaAs), reveals critical insights into their performance metrics, quantum transport behavior, and carrier scattering mechanisms. The findings underscore the limitations of traditional silicon-based CMOS technology as devices scale below 10 nm, highlighting the need for alternative channel materials to sustain the performance trajectory dictated by Moore's Law. InGaAs emerged as the most promising candidate for nMOSFET applications, demonstrating exceptionally high electron mobility, minimal scattering effects, low subthreshold swing, and superior drive current capabilities. Meanwhile, Ge proved to be the ideal material for pMOSFETs, offering excellent hole mobility, moderate scattering rates, and reliable thermal stability. SiGe, while offering moderate improvements over pure silicon, fell short in terms of carrier mobility and scattering performance when compared to InGaAs and Ge. These findings are consistent with previous research studies by Chau *et al*. [3], Takagi *et al*. [2], and Fischetti *et al*. [14], further validating the robustness of the results presented here.

One of the critical observations was the strong correlation between carrier mobility, scattering mechanisms, and drive current, as validated by ANOVA and Tukey post-hoc statistical tests. InGaAs exhibited the lowest scattering rates across phonon, surface roughness, and Coulomb interactions, making it highly efficient for next-generation nMOSFETs. Ge's moderate scattering rates further reinforce its suitability for pMOSFET applications. However, the successful integration of these materials into mainstream CMOS manufacturing remains challenging due to factors such as lattice mismatch, defect densities, and thermal instability at nanoscale dimensions. The results from the quantum transport simulations, validated through NEGF modelling, provided a detailed understanding of electron and hole dynamics within ultra-scaled devices, strengthening the hypothesis that optimized material composition and structural properties can effectively mitigate scattering effects and enhance carrier transport.

Practical Recommendations

Practical recommendations based on this study emphasize the importance of a heterogeneous integration approach for future CMOS technology. Specifically, it is recommended that InGaAs be adopted as the channel material for nMOSFETs and Ge for pMOSFETs in sub-10 nm devices. This dual-material approach will leverage the strengths of each material, maximizing overall CMOS performance. Additionally, device fabrication processes must focus on minimizing interface defects and optimizing gate dielectric interfaces to fully exploit the transport potential of these materials. Advanced deposition techniques, such as molecular beam epitaxy (MBE) and atomic layer deposition (ALD), should be prioritized to ensure uniform and defect-free material layers. Thermal stability, particularly at elevated operating voltages, must also be addressed through innovative device architectures, such as gate-all-around (GAA) structures and strain-engineered channels, to maintain reliability over prolonged operation.

On the computational front, continued advancements in quantum transport simulations using NEGF formalism and hybrid modelling techniques should be pursued to predict device behaviour under varying conditions more accurately. Statistical tools like PCA, which highlighted electron mobility and scattering rates as dominant performance drivers, should be systematically incorporated into future studies for performance optimization and material screening. Furthermore, investment in advanced metrology tools such as high-resolution TEM, SIMS, and EDS is essential for accurate characterization and validation of material properties at the atomic scale.

Collaboration between academia, semiconductor industries, and material science laboratories will be crucial in addressing the integration challenges and accelerating the commercial deployment of these materials. Additionally, government and private funding initiatives should prioritize research on novel materials, fabrication techniques, and device architectures to ensure technological readiness for future CMOS nodes.

In conclusion, this study establishes InGaAs and Ge as the leading candidates for nMOSFET and pMOSFET channel materials, respectively, offering clear advantages over traditional silicon technology. However, their successful integration into large-scale manufacturing demands focused efforts on mitigating defect densities, optimizing material interfaces, and refining fabrication techniques. Future research should also explore the potential of hybrid channel architectures, multi-material integration, and emerging two-dimensional (2D) materials to push the boundaries of CMOS technology further. With strategic alignment between research, industry, and policy support, these advancements can pave the way for highly efficient, energy-saving, and scalable semiconductor devices, ensuring the continued evolution of digital technology in the post-silicon era.

References

1. Moore GE. Cramming more components onto integrated circuits. Electronics. 1965;38(8):114-117.
2. Takagi S, Hoyt JL, Welser JJ, Gibbons JF. Comparative study of phonon-limited mobility in strained and unstrained Si MOSFETs. IEEE Trans Electron Devices. 1996;41(12):2357-2362.
3. Chau R, Doyle B, Datta S, Kavalieros J, Zhang K. Integrated nanoelectronics for the future. Nat Mater. 2007;6(11):810-812.
4. Lee CH, Zhu W, Nishimura T, *et al*. Germanium MOSFETs: The future of high-performance logic devices. IEEE Electron Device Lett. 2011;32(5):556-558.
5. Franklin AD. Nanomaterials in transistors: From high-performance to thin-film applications. Science. 2015;349(6249):aab2750.
6. Kim HS, Choi CH, Lee SW, *et al*. Strained SiGe channels for high-mobility CMOS. J Appl Phys. 2008;103(8):083703.
7. Ren Z, Lundstrom MS, Datta S. Ballistic transport in nanoscale MOSFETs. IEEE Trans Electron Devices. 2001;47(7):1257-1264.
8. Li D, Mleczko MJ, Hu C, Pop E. Opportunities for two-dimensional electronics in beyond-CMOS logic. Nat Commun. 2018;9:456.
9. Connelly D, Duane R. Challenges in integrating III-V channel materials into CMOS. Appl Phys Lett. 2008;93(9):092107.
10. Iwai H. Roadmap for 22 nm and beyond. Microelectron Eng. 2009;86(7-9):1520-158.
11. Jena D. Tunneling transistors based on graphene and 2D crystal semiconductors. Proc IEEE. 2013;101(7):1585-1608.
12. Riel H, Wernersson LE, Hong M, del Alamo JA. III-V compound semiconductor transistors—from planar to nanowire structures. MRS Bull. 2014;39(8):668-677.
13. Datta S. Quantum Transport: Atom to Transistor. Cambridge University Press; c2005.
14. Fischetti MV, Neumayer DA, Cartier EA. Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-kappa insulator: The role of remote phonon scattering. J Appl Phys. 2001;90(9):4587-4608.
15. Jin S, Fischetti MV, Tang T. Modeling of electron mobility in strained Si/SiGe MOSFETs. IEEE Trans Electron Devices. 2007;54(9):2191-2200.
16. Lundstrom MS. Fundamentals of Carrier Transport. Cambridge University Press; c2000.
17. Dargis R, Ouellet M, Savoia M, *et al*. Carrier scattering mechanisms in ultra-thin-body MOSFETs. Solid-State Electron. 2012;74:53-62.
18. Islam MS, Alam MA. Atomistic simulation of phonon

scattering in nanoscale transistors. IEEE Trans Nanotechnol. 2009;8(2):244-250.
19. Palestri P, Esseni D, Selmi L, *et al*. Analysis of low-field mobility in nMOS transistors with high-kappa gate dielectrics. IEEE Trans Electron Devices. 2008;55(8):2081-2090.
20. Ferry DK, Goodnick SM. Transport in Nanostructures. Cambridge University Press; c 1997.
21. Yang Z, Chen Y, An J, *et al*. Performance and variability of ultra-thin body III-V MOSFETs. Appl Phys Lett. 2013;102(8):083503.