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Switching scheme of voltage levels and logic equation in asymmetrical single-phase seven-level cascaded H-bridge multilevel inverter

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Abstract
The development of multilevel inverters has made it easier to extract power from direct current sources to alternating current power. This journal presents the switching scheme of voltage levels and logic equations in asymmetric single-phase seven-level cascaded H-bridge multilevel inverter. The minimum switching logic circuit for the single phase seven-level cascaded H-bridge multilevel inverter was obtained by modelling the logic equations that could be used with any number of levels depending on the number of modulating and carrier signals involved. The logic equations have made it easier to design with phase disposition pulse width modulation or any carrier signal for cascaded H-bridge multilevel inverter and the logic gates designed to give an optimum harmonic value.

Keywords: multilevel inverter, switching schemes, logic equations

Introduction
The asymmetric single-phase seven-level Cascaded H-bridge multilevel inverter has two dc sources and six power switches and the magnitude of input dc voltage sources of $100V_{dc}$ and $200V_{dc}$. The output voltage can be positive voltage ($+V_{dc}$), Zero voltage ($0V_{dc}$) and Negative voltage ($-V_{dc}$). Hence the desired voltage levels for seven-level asymmetric cascaded H-bridge multilevel inverter are from $+3V_{dc}$ to $-3V_{dc}$. In considering the switching sequence and logic equations of a single-phase seven-level cascaded H-bridge multilevel inverter, it is important to focus on the switches only and their reduction. To obtain voltage levels of multilevel inverter, single-phase seven-level is adopted. Various research works are going on over inverter circuit configuration mainly in reducing the switches at higher voltage level. In such arrangements, dc battery sources supply dc voltages that differ in a wide range according to different load conditions. Further by reducing switches and increasing level will reduce cost and harmonic content. Single-phase seven-level cascaded H-bridge multilevel inverter topology requires twelve switches but in this paper, the switches are reduced from twelve to six, in which the same multilevel output voltage is obtained. Invariably switching losses and cost are also reduced. In reality a high step up converter is used before inverter input circuit for maintaining high constant voltage. In this paper we are going to study only about multilevel inverter switching sequence and logic equations in their circuitry.

Switching Schemes of Voltage Levels in Seven-level Cascaded H-bridge Multilevel Inverter
Power electronic converters are operated in the "switched mode" [3]. Which means the switches within the converter are always in either one of the two states, turned off (no current flows) or turned on (saturated with only a small voltage drop across the switch) [1]. From Figure 1 and Table 1, $+3V_{dc}$ voltage level was obtained by switching on switch S_6, S_2, and S_4, while switch S_3, S_1 and S_5 are switched off. $+2V_{dc}$ voltage level was obtained by Switching on switch S_6, S_2 and S_1, while switch S_3, S_4 and S_5 are switched off. $+1V_{dc}$ voltage level was obtained by Switching on switchS_3, S_2 and S_4, while switch S_6, S_1 and S_5 are switched off. $0V_{dc}$ voltage level was obtained by switching on Switch S_6, S_5 and S_4 while switch S_3 , S_2 and S_1 are switched off. $-1V_{dc}$ voltage level was obtained by switching on switch S_1, S_5 and S_6, while switch S_4, S_2 and S_3 are switched off. $-2V_{dc}$ voltage level was

obtained by Switching on switchS_4, S_5 and S_3, while switch S_1, S_2 and S_6 are switched off.. -3V_{dc} voltage level was obtained by switching on switch S_1, S_5 and S_3, while switch S_4, S_2 and S_6 are switched off. All these were summarily presented in table 1 [2].

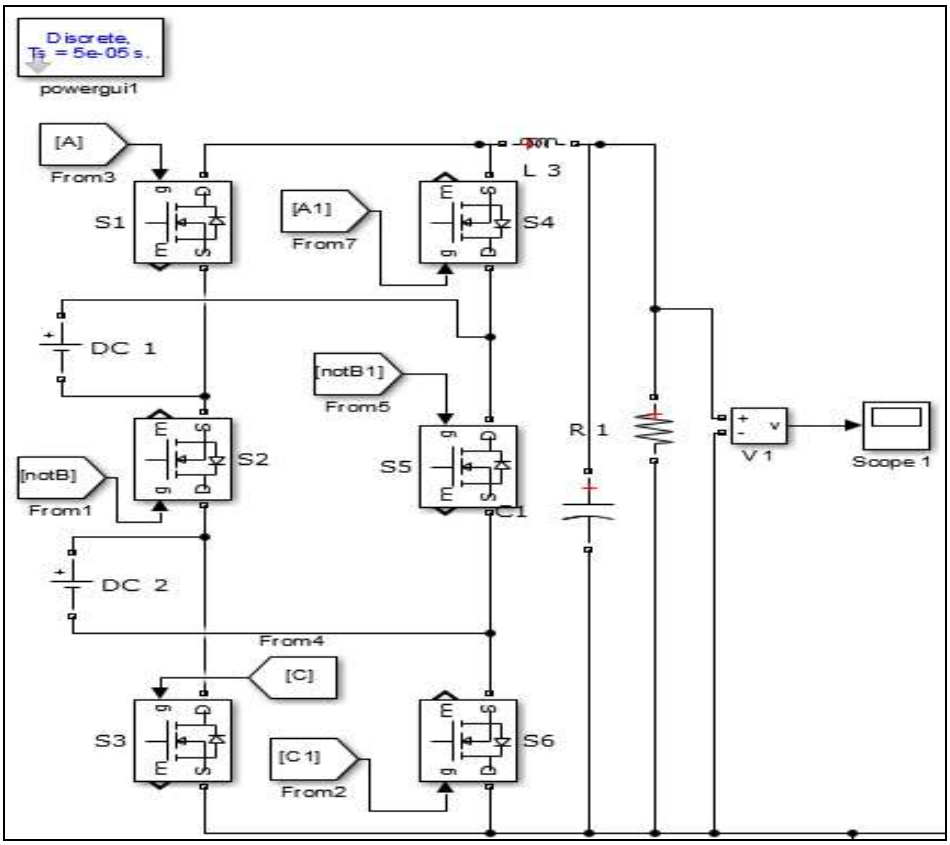


Fig 1: Circuit diagram of single-phase seven-level cascaded H-bridge multilevel inverter

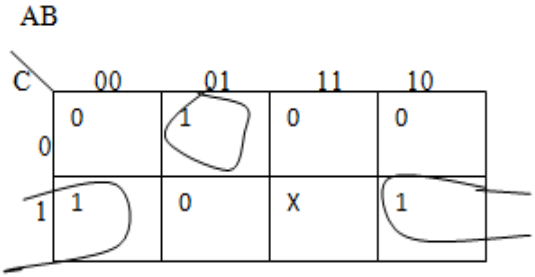
Table 1: Switching states for single-phase asymmetric seven-level cascaded H-bridge Multilevel inverter with reduced number of switches

s/n	Switching sequences						Voltage levels
	S_1	S_2	S_3	S_4	S_5	S_6	(V_{dc})
1	0	1	0	1	0	1	+3
2	1	1	0	0	0	1	+2
3	0	1	1	1	0	0	+1
4	0	0	0	1	1	1	0
5	1	0	0	0	1	1	-1
6	0	0	1	1	1	0	-2
7	1	0	1	0	1	0	-3

Note; **1** denoted that switches are ON state, while **0** denoted that switches are OFF

Switching Logic Equations

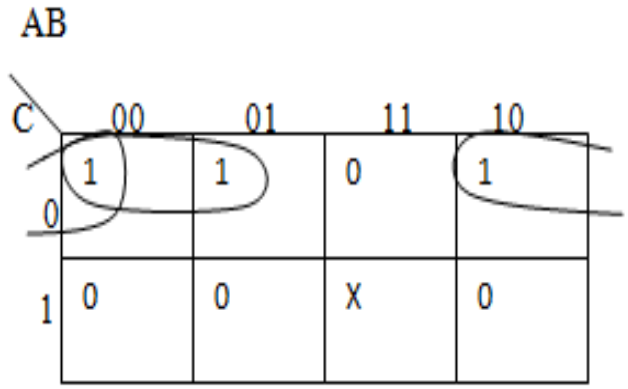
The operation of a single-phase seven level cascaded H-bridge multilevel inverter with reduced number of switches requires six carrier signals and a reference waveform combine to produce pulses which turn ON and OFF the inverter using phase disposition (PD) sinusoidal pulse width modulation (SPWM). The switches of this cascaded H-bridge multilevel inverter are numbered from S_1 to S_6 as shown in Figure 1. The logic equations based on the result of the switching sequences from Table 1 which give rise to the simplified sequential equations with the uses of karnaugh map. For switch S_1 to switch S_6 the Sum of product are, F (A, B, C) = ∑m (0, 1, 2, 3, 4, 5 and 6) and seven is don't care (x) and these were represented in karnaugh map for S_1 to S_6 in Figure 2 to Figure 7 [4], [5]



S_1 = F (A, B, C) = ∑m (1, 4, 6)

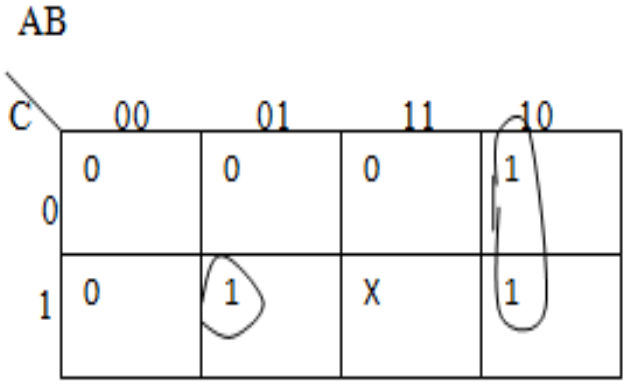
F = $\overline{A}$ B$\overline{C}$ + $\overline{B}$C

Fig 2: Karnaugh for S_1



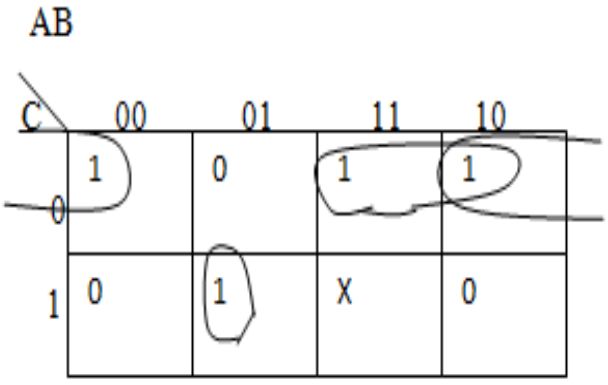
S_2 = F (A, B, C) = ∑m (0, 1, 2),
F = $\overline{AC}$ + $\overline{B}\overline{C}$

Fig 3: Karnaugh for S_2



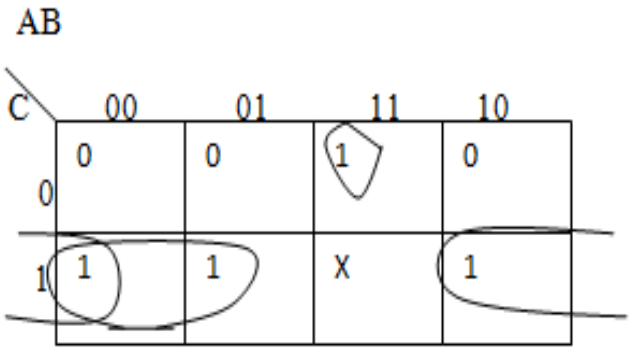
S_3 = F (A, B, C) = ∑m (2, 5, 6),
F = $\overline{A}$BC + A$\overline{B}$

Fig 4: Karnaugh for S_3



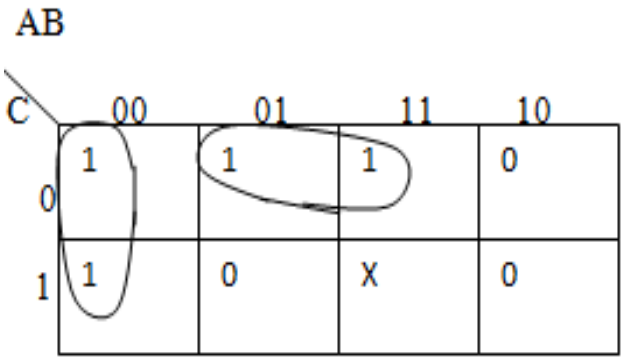
S_4 = F (A, B, C) = ∑m (0, 2, 3, 5),
F = $\overline{B}\overline{C}$ + A$\overline{C}$ + $\overline{A}$BC

Fig 5: Karnaugh for S_4



S_5 = F (A, B, C) = ∑m (3, 4, 5, 6)
F = $\overline{A}$C + $\overline{B}$C + AB$\overline{C}$

Fig 6: Karnaugh for S_5



S_6 = F (A, B, C) = ∑m (0, 1, 3, 4), F = $\overline{AB}$ + B$\overline{C}$

Fig 7: Karnaugh for S_6

The Boolean expressions from the karnaugh map above are summarized below.

S_1 f= $\overline{A}$B$\overline{C}$ + $\overline{B}$C (1)

S_2 = $\overline{AC}$ + $\overline{B}\overline{C}$ (2)

S_3 = $\overline{A}$BC + A$\overline{B}$ (3)

S_4 = $\overline{B}\overline{C}$ + A$\overline{C}$ + $\overline{A}$BC (4)

S_5 = $\overline{A}$C + $\overline{B}$C + AB$\overline{C}$ (5)

S_6 = $\overline{AB}$ + B$\overline{C}$ (6)

Where A, B and C are signals that generate pulses for the cascaded H-bridge multilevel inverter. The logic circuit is designed based on the switching pattern of the six switches in the reduced number of switches of single phase seven-level cascaded H-bridge inverter and modelled equations. The logic circuit is shown in Figure 8.

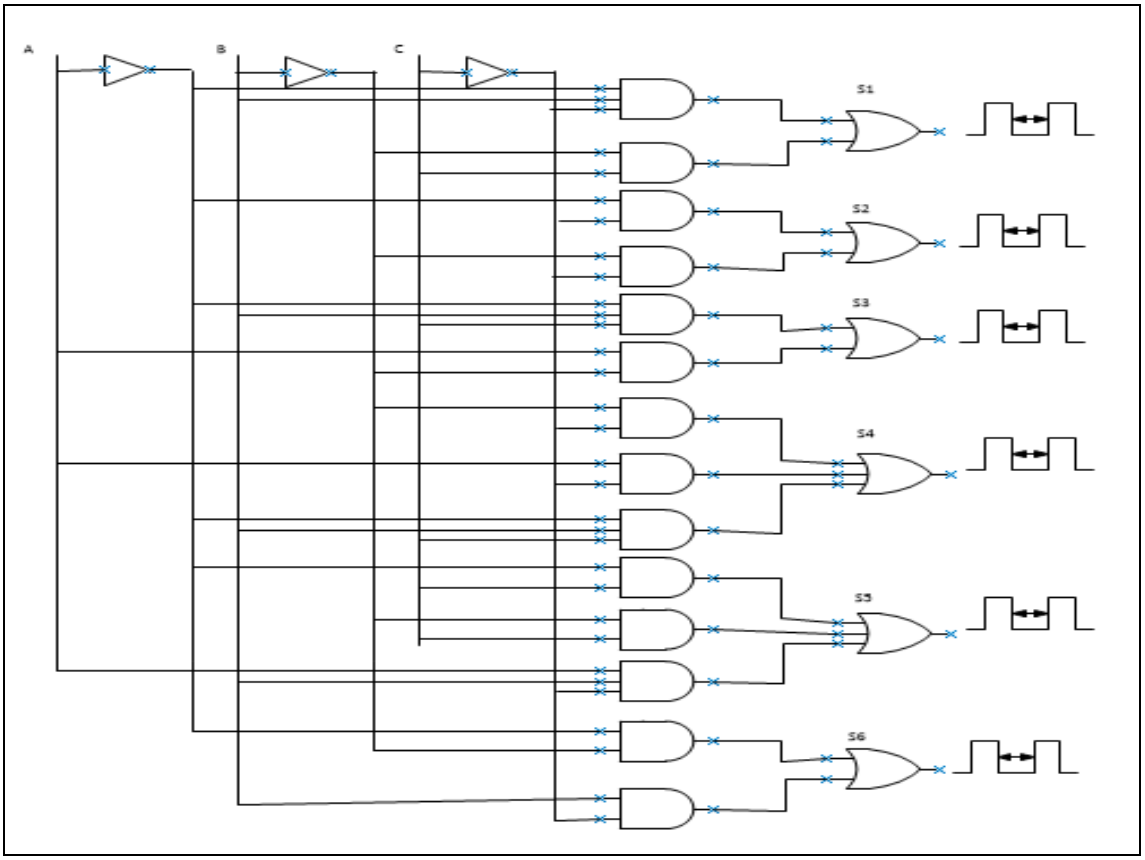


Fig 8: Logic circuit

Principle of PWM Generation of Three Phase CHB MLI Inverter

The control block is essentially the pulse width modulation circuit which consists of an aggregate of a reference sine wave generator (Phase shift oscillator), a triangular carrier wave generator (integrator) and a comparator (modulator). The sine wave is the reference signal and is compared with the triangular signal to produce a modulated output that is used to drive the power circuit. Different modulation methods are used to generate the staircase output of the H-bridge inverter. The circuit diagram of the principle of generation pulse width modulation is shown in Figure 9 [6].

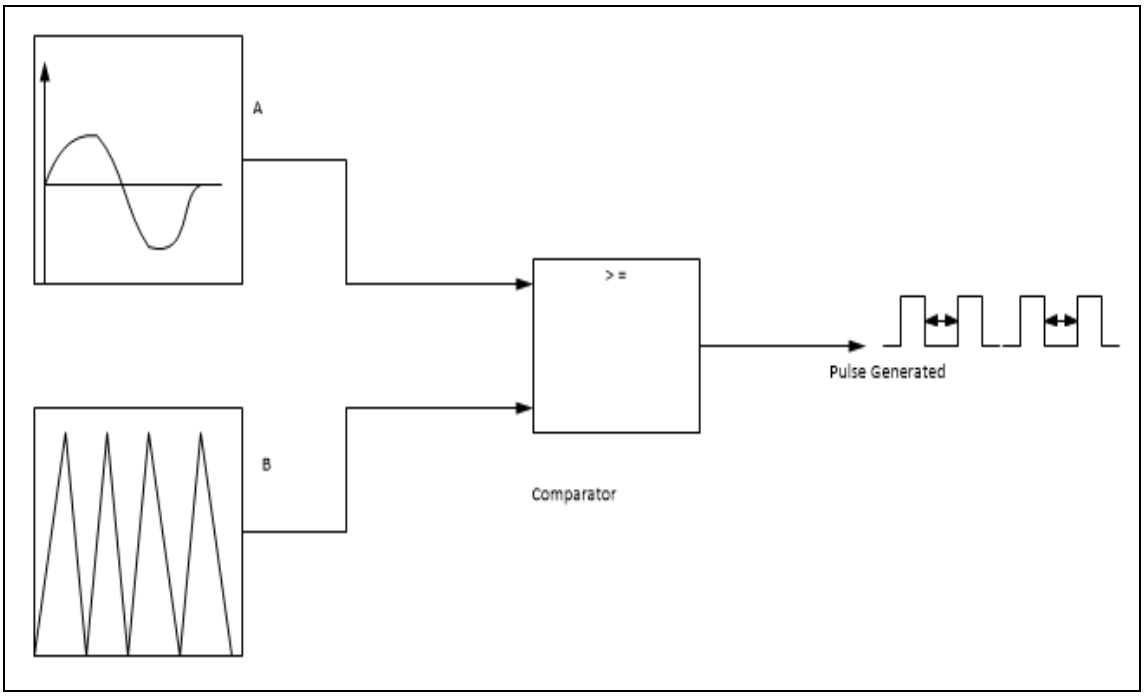


Fig 9: Principle of PWM generation

Where A is a reference carrier signal and B is a triangular carrier signal from figure 19. If A > B signal will be generated, if A = B signal will be generated. But if A< B no signal will generate.

Conclusion

The phase disposition pulse width modulation logic gate circuit uses six OR, fourteen NAND and three NOT gates based on the derived equations to produce pulses for the seven-level multilevel inverter. The logic equations have made it easier to design a modulation circuit for a cascaded H-bridge multilevel inverter with any number of levels using phase disposition pulse width modulation or other carrier signals.

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